45th IEEE International Midwest Symposium on Circuits and Systems

Conference Program

August 4-7, 2002

Tulsa, Oklahoma

Co-Sponsored by the IEEE Circuits and Systems Society and the School of Electrical and Computer Engineering at Oklahoma State University

For the latest information please visit the Symposium website:
www.mwscas2002.org

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Message from the 45th MWSCAS Co-Chairs

Welcome to the 45th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS-2002) to be held on the Tulsa campus of Oklahoma State University August 4-7, 2002. The conference hotel is the Adam's Mark Hotel of Tulsa. This year's conference is co-sponsored by the IEEE Circuits and Systems Society and the School of Electrical and Computer Engineering at Oklahoma State University. This is the second time that the School of Electrical and Computer Engineering at Oklahoma State University has hosted the conference; however, the last time was the 9th symposium held in 1966, 36 years ago. Oklahoma State University is proud to be one of only six universities to host the conference more than once (the other five are: University of Illinois, Iowa State University, Michigan State University, Notre Dame and University of Wisconsin).

We are very excited about the technical program for this year's conference. Over 575 papers were submitted to the conference including 193 papers submitted to the sixth annual MWSCAS Student Paper Contest. From the 193 papers submitted to the student paper contest, ten presenters and two alternates were chosen to present their papers Monday morning in the Student Paper Contest. This is an outstanding honor considering that only 5% of the papers submitted are selected for the contest. Many of the other papers have been scheduled in regular sessions – so all of the outstanding student papers will be presented at the conference even though we can only showcase ten of them. Complete details on the technical program can be found in the message from the Technical Program Chair Keith Teague.

While the technical program is certainly the core of MWSCAS, this year's symposium boasts several venues that add value to the conference. At the opening session on Monday morning, OSU-Tulsa President Gary Trennepohl and Dean Karl N. Reid will welcome everyone to OSU-Tulsa and to the symposium. Keynote addresses on Tuesday by Williams Communications Group C.E.O Howard Janzen and on Wednesday by Transmeta C.E.O. Matthew Perry will set the events for each day. We are fortunate to have Paul Kolodzy, the newly named chair of the Federal Communications Commission (FCC) Task Force on Spectrum Policy, organize and chair a panel discussion on the "Future of Telecom" at a Wednesday luncheon. In addition, special invited talks are scheduled each day. MWSCAS will also host the IEEE Tri-State Conference on Sunday and the IEEE North America Chairs meeting on Tuesday in parallel with a great set of tutorials and short courses that will be offered all day Sunday. In addition to the great technical program, we will have exhibits everyday in Room 151 (Roberts Room) and a Career Fair on Tuesday afternoon in the atrium of Main Hall.

We have also arranged for several technical and social tours. These include technical tours to Williams Communications, ABB, Flight Safety International and the Oklahoma State University main campus in Stillwater. Social tours will include Frankoma Pottery, Woolaroc Museum, The Oklahoma City National Memorial, and the Philbrook and Gilcrease museums. Social events include a reception on Sunday evening in the Ballroom of the Adam's Mark Hotel, the awards luncheon on Monday that will include the awarding of the Myril B. Reed Best Paper Award from last year's conference and the awarding of the first, second and third place winners in the student paper contest. For those on the MWSCAS Steering Committee, this year's meeting and dinner will be on Monday at 6:30 pm in the Adam's Mark Hotel.

This symposium would not be possible without all of the authors who contributed papers to the technical program, the many volunteers that assisted with the technical program and with the conference organization, and the strong support of the many industrial and corporate sponsors who have given time, energy and money to support this symposium. We have tried to list all those who have contributed in the pages that follow, but so many contributed that it is not possible to recognize everyone. However, on behalf of the MWSCAS Conference Committee, we would like to thank all who contributed to the conference.

Please enjoy your stay in Tulsa and the many events associated with the conference. If time permits, we hope you will be able to explore Tulsa and Oklahoma while you are at the symposium. Tulsa is a wonderful city with many things to see and do. The MWSCAS web site lists a few of these. We sincerely hope you will enjoy your stay in Tulsa.

Michael A. Soderstrand and Rao Yarlagadda
Oklahoma State University

Technical Program Chair's Message

Welcome to Tulsa and the 45th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS-2002). I am very pleased you have chosen to attend, and I believe you will agree that this year's program is excellent. This is certainly a tribute to the high quality of the submissions, an excellent Technical Program Committee, and the many fine track and session chairs who have contributed their time and energy to organizing this year's Symposium. I hope you find the program stimulating and entertaining, and you enjoy your visit to Oklahoma.

This year's Symposium was organized with ten technical tracks, and nominally eleven technical sessions per track. These numbers varied based on the relative frequency of submissions, with Analog Circuits and Systems representing the largest track. This year's technical tracks, and the corresponding track chairs are:

- Analog Circuits and Systems (John Choma and Randy Geiger)
- Digital Circuits and Computer Arithmetic (Magdy Bayoumi)
- Programmable Logic, VLSI, CAD and Layout (Linda DeBrunner)
- Communications Networking (J-M Chung)
- Wireless Communications Systems (Michael Buehrer)
- Neural Networks and Control Systems (Martin Hagan)
- Digital Signal Processing (Victor DeBrunner)
- Digital Signal Analysis (Scott Acton)
- Power and Energy Systems and Power Electronics (Ward Jewell)
- RF, Microwave and Optical Circuits and Systems (James West)

All submitted papers were reviewed by session chairs and members of the Technical Program Committee. No distinction was made between lecture and poster submissions. A final decision on each paper was rendered at the Technical Program Committee meeting in June.

We have an exceptionally strong schedule of technical events planned this year. In addition to more than 500 paper presentations in 111 technical sessions, we are very fortunate to have special keynote addresses and invited presentations each day, plus an extraordinary panel discussion and luncheon, "The Future of Telecom", which will be held at the Greenwood Cultural Center adjacent to the OSU-Tulsa campus on Wednesday. On Monday, Terry Alderson of Boeing Wichita Division will deliver an invited talk titled "RFID Implementation". Tuesday morning John Worden of Seagate Technology will discuss "The Serially Attached SCSI (SAS) Interface", followed on Tuesday afternoon by Clifford Lau of the Office of Naval Research who will present a one-hour in-depth talk on "ONR/DOD Research Programs in Nanotechnology". The invited talks will conclude on Wednesday with Mathew Oommen, C.T.O. of Optical Datacom, who will discuss "Telecom Infrastructure Issues". It's very gratifying that these speakers have chosen to take time from their busy schedules to be with us at MWSCAS-2002.

The sixth annual MWSCAS Student Paper Contest will be held in its own session on Monday morning. During this special lecture session, the top ten student papers as determined by a special student paper contest committee chaired by Rick Branner will be presented. Be sure to attend and show your support for all the participants! The winners of this year's MWSCAS Student Paper Contest will be recognized and prizes awarded at the Awards Luncheon following the session. Also at the luncheon on Monday, the annual Myril B. Reed Best Paper award will be presented for 2001.

Thank you for your contributions and attendance at MWSCAS-2002. Through your participation attending sessions, submitting and presenting papers, serving as a session chair or on the Technical Program Committee, volunteering to help with activities at the Symposium, or by serving as a Symposium Sponsor, you have helped make this year's conference a huge success. I hope you have a wonderful time in Tulsa!

Keith A. Teague
Oklahoma State University

MWSCAS-2002 Program Committee

General Co-Chairs
Michael A. Soderstrand
Oklahoma State University
sodersm@okstate.edu

Rao Yarlagadda
Oklahoma State University
yar@okstate.edu

Technical Program Chair
Keith A. Teague
Oklahoma State University
teague@okstate.edu

Tutorials
Ken Jenkins
Pennsylvania State University
jenkins@engr.psu.edu

Student Paper Contest
Rick Branner
University of California-Davis
branner@ece.ucdavis.edu

Finance and Administration
George Collington
Oklahoma State University
gcollin@okstate.edu

Publicity
Carl Latino
Oklahoma State University
latino@okstate.edu

Registration
C.J. Behrenbrinker
Oklahoma State University
cath@okstate.edu

Corporate Sponsorship
Marc Thompson
Oklahoma State University
mthompson@okstate.edu

Ron Cooper
Center for Excellence in Information and Telecommunications Technology (COEITT)
rcooper@osu-tulsa.okstate.edu

Publications Coordinator
Tom Wehner
Alliance Management Group
t.wehner@ieee.org

Technical Track Chairs
Analog Circuits and Signal Processing
John Choma, Jr.
University of Southern California
johnc@usc.edu

Randy Geiger
Iowa State University
rlgeiger@iastate.edu

Digital Circuits and Computer Arithmetic
Magdy Bayoumi
mbayoumi@cacs.louisiana.edu

Programmable Logic, VLSI, CAD and Layout
Linda DeBrunner
University of Oklahoma
ldebrunner@ou.edu

Communications Networking
Jong-Moon Chung
Oklahoma State University
jchung@okstate.edu

Wireless Communications Systems
Michael Buehrer
Virginia Tech University
buehrer@vt.edu

Neural Networks and Control Systems
Martin Hagan
Oklahoma State University
mhagan@okstate.edu

Digital Signal Processing
Victor DeBrunner
University of Oklahoma
vdebrunn@ou.edu

Digital Signal Analysis
Scott Acton
University of Virginia
acton@virginia.edu

Power and Energy Systems and Power Electronics
Ward Jewell
Wichita State University
ward.jewell@wichita.edu

RF, Microwave and Optical Circuits and Systems
Jim West
Oklahoma State University
jwest@okstate.edu

Local Arrangements
Marsha Hayes
Oklahoma State University
mhays@osu-tulsa.okstate.edu

Exhibits
Rao Yarlagadda
Oklahoma State University
yar@okstate.edu

George Collington
Oklahoma State University
gcollin@okstate.edu

Kami Schieber
Oklahoma State University
kamishawn@hotmail.com

Tours and Special Events
Lory Ferguson
Oklahoma State University
fergusa@okstate.edu

Career Fair
Carolyn Miller
Oklahoma State University
cjmill@okstate.edu

Volunteer Coordinators
Shyam Uma Chandra
Christine Co
Janna Nowisczski

IT Support and Email Center
Alan Hall
Oklahoma State University
hallad@okstate.edu

OSU/Williams Telecom Teaching and Research Lab
Mark Weiser
weiser@okstate.edu

George Scheets
scheets@okstate.edu

J. M Chung
jchung@okstate.edu

IEEE Multi-Section Region V Meeting

What started as a Tri-State IEEE Section meeting planned in conjunction with the IEEE Midwest Symposium is being expanded to a Regional meeting. Robert Scolli, Region 5, North Area Chair, is expecting representation from the following sections: Tulsa, Oklahoma City, Wichita, Ozark (Fayetteville), Kansas City, Arkansas River Valley, Shreveport, Dallas and Ft Worth Sections.

This multi-sectional meeting will present a rare opportunity for the different regional IEEE sections to meet and get to know each other better by exchanging information on professional and regional activities.

Prior to the meeting, a tour is scheduled of OSU-Tulsa campus's newly unveiled Telecommunications and Information Technology Teaching Research Laboratory, which will also serve as the MWSCAS conference e-mail center. Brought online this spring, the laboratory is tied to facilities in Stillwater and throughout the state via a direct fiber link to support collaboration between the campuses and distance education worldwide. The laboratory is located in Room 1308 Main Hall.

"It is truly the premier telecommunications research laboratory facility; there's no other teaching facility in the world that has better equipment and capabilities," says Dr. Michael Soderstrand, MWSCAS Conference Co-chairman and Head of OSU's School of Electrical and Computer Engineering.

A presentation on "Progress and Status of Hybrid Electric Vehicles (HEVs)" will be made by Robert Strattan, P.E., a Senior Life Member of the IEEE, Emeritus Professor of Electrical Engineering at the University of Tulsa, and currently Vice-chair of the IEEE Tulsa Section.

The presentation will describe the objectives and characteristics of HEVs, experiences of a daily driver of HEV vehicles, and project what lies in the future as electrical drive-line components become more integrated into our automobiles.

The Hurricane Motor Works, a University of Tulsa Lab where students are working on their third generation of HEVs, is located at the Tulsa University's North Campus research facility. A tour of the Hurricane Motor Works is scheduled following the formal meeting.

MWSCAS 2002 Tutorials
Sunday August 4, 2002, 9:00 am – 5:00 pm

MWSCAS 2002 continues the tradition of providing cutting-edge short courses and tutorials on the Sunday before the conference. This year we have four short courses and tutorials available that include:

1. Edward J. Delp, Purdue University, *Digital Watermarking* (Full Day)
2. Scott C. Douglas, Southern Methodist University, *Blind Source Separation: Criteria, Methods, and Applications* (Full Day)
3. Susan Chinburg, Janice Hanson and Vincent Chong, Williams Communications Group, *Network Planning and Traffic Engineering using Modeling and Simulation Processes, a Systems Approach for the Entire Network* (Half Day)
4. Gabriel A. Rincon-Mora, *Integrated DC-DC Converters: A Topological Journey!* (Half Day)

Continuing Education Units (CEUs) are available both for the tutorials and technical sessions. Additional information is available at the MWSCAS registration desk and is included in your registration packet.

MWSCAS Opening Session
Monday August 5, 2002, 8:00 am – 8:20 am

As is the custom at MWSCAS, the opening session is planned to be short and to the point. We are pleased to have all of you here at OSU-Tulsa attending the 45th IEEE MWSCAS. To celebrate this event, Dr. Gary Trennepohl, President of Oklahoma State University-Tulsa will welcome everyone to OSU-Tulsa. Dr. Gary Trennepohl became the first President of Oklahoma State University-Tulsa on Sept. 1, 1999. He was formerly Dean of the College of Business Administration at Oklahoma State University in Stillwater. Trennepohl, 55, previously held faculty and administrative appointments at Texas A&M University (1986-1995, executive associate dean and Peters Professor of Finance), the University of Missouri-Columbia (1982-1986, professor and finance department chair), and Arizona State University (1977-1982, associate professor).

After the welcome by President Trennepohl, Dr. Karl N. Reid, Dean of the College of Engineering, Architecture and Technology of Oklahoma State University will provide a warm welcome from the College to all the MWSCAS attendees. Dean Reid has been Dean of the College since 1986 and is a graduate of Oklahoma State University and received his Ph.D. from Massachusetts Institute of Technology. He formerly was the head of the School of Mechanical and Aerospace Engineering at Oklahoma State University. Dean Reid is the founder of The Web Handling Research Center (WHRC) at OSU, which is one of fifty-two National Science Foundation Industry/University Cooperative Research Centers. The WHRC was initiated in 1986 and is the only center of its type in the world.

MWSCAS Student Paper Contest
Chair: Rick Branner
Monday August 5, 2002, 8:20 am – 12:00 Noon

The 45th IEEE International Midwest Symposium on Circuits and Systems will host the sixth annual MWSCAS Student Paper Contest. Nearly 200 papers were submitted from all over the world to compete in the first round of the contest in which ten contestants and two alternates were chosen to compete in the oral portion of the contest. The ten contestants scheduled to compete from 8:20 am to 12 Noon in the main auditorium at OSU-Tulsa are:

1. *Zhangwen Tang,* "High-Performance All-Digital Quadrature Frequency Synthesizer/Mixer", Fudan University, Shanghai, China
2. *Sebastian Magierowski,* "Nonlinear Analysis of CMOS LC-Tuned VCO Phase Noise", University of Toronto, Toronto, Canada
3. *Chuang Zhang, "*A 0.8V Ultra-low Power CMOS Operational Amplifier Design", Louisiana State University, Baton Rouge, LA, USA
4. *Masoud Karimi-Ghartemani, "*A Novel System for Measurement of Power System Parameters and Signals", University of Toronto, Toronto, Canada
5. *Enjun Xiao, "*RF Circuit Performance Degradation Due to Hot Carrier Effect and Soft Breakdown", University of Central Florida, Orlando, FL, USA
6. *Jeevan Chittamuru,* "An Adaptive Low Power Texture Mapping Architecture for 3D Graphics", University of Massachusetts, Amherst, MA, USA
7. *Mourad El-Gamal,* "Micro-Electromechanical Variable Capacitors for RF Applications", McGill University, Montreal, Canada
8. *Erik Backenius,* "A Strategy for Reducing Clock Noise in Mixed-Signal Circuits", Linkoping University, Linkoping, Sweden
9. *Anthony Long,* "A 13W Current Mode Class D High Efficiency 1 GHz Power Amplifier", University of California, Santa Barbara, CA, USA
10. *Biju Mullul Veedu,* "Simple Adaptive Heterodyne Filter", Oklahoma State University, Stillwater, OK, USA

The two alternates will present only if one of the ten above are unable to travel to present their papers at the conference. Nonetheless, being selected as an alternate out of nearly 200 papers submitted is quite an honor. All ten contestants and the two alternates will receive free registration and accommodations and assistance with their travel expenses. In addition, they will all receive certificates of selection for the contest. The two alternates are:

1. *Omar Elkeelany,* "A Prototype of WideBand/Ethernet Bridge using WEMAC", University of Missouri, Kansas City, MO, USA
2. *John Condren,* "Eigenvalue and Eigenvector Sensitivities Applied to Power System Steady-State Operating Point", Oklahoma State University, Stillwater, OK, USA

Keynote Speaker
Tuesday August 6, 8:00 am – 9:00 am
OSU-Tulsa Auditorium, North Hall

Howard E. Janzen
Chairman, President & Chief Executive Officer
Williams Communications
"Telecom Market Place: A View from the Top"

Howard E. Janzen is chairman, president and chief executive officer of Williams Communications. Janzen has led Williams Communications in completing the largest next-generation fiber network in the U.S. The network has attracted a high-quality portfolio of bandwidth-centric customers who have committed to the Williams Communications network as their broadband enabler.

A recognized leader in the telecommunications industry, Janzen received the 2001 Ovations award from *Tele.com* magazine and COMNET for the company's extraordinary achievements in technology and operations. Under Janzen's guidance, Williams Communications' network has been awarded SuperQuest's "Best Built Core Backbone" for an unprecedented three consecutive years (1998-2000).

Janzen has 25 years experience in the telecommunications and energy industries. His career with former parent Williams began as a project engineer for Williams Pipe Line in 1979, and he has served in numerous management positions in the Energy and Gas Pipeline businesses during his 22 years. He was named head of the new Communications business unit formed in 1995 and became president and chief executive officer of Williams Communications Group in April 1997, which became an independent company in April 2001.

Janzen earned Bachelor of Science and Master of Science degrees in Metallurgical Engineering from The Colorado School of Mines and is a licensed Professional Engineer. He has also completed the Harvard Business School Program for Management Development. Janzen became a Colorado School of Mines Distinguished Achievement Medalist in 1996.

Janzen serves on the Board of Trustees at The University of Tulsa, the Bank of Oklahoma Board of Directors and on the Board of Trustees for the Hillcrest Healthcare System. He also serves on the Governor's Science & Technology Council for the State of Oklahoma and is a Commissioner for the Global Information Infrastructure Commission (GIIC). He serves on the Gilcrease Museum Board of Directors and is co-chairman of the Resources Campaign for The Colorado School of Mines. Janzen was recently inducted into the University of Tulsa, College of Engineering and Natural Sciences, Hall of Fame.

Keynote Speaker
Wednesday August 7, 8:00 am – 9:00 am
OSU-Tulsa Auditorium, North Hall

Matthew R. Perry, Ph.D.
President & Chief Executive Officer
Transmeta Corporation
"Mobile Computing"

Matt Perry joined Transmeta in April 2002 as President, Chief Executive Officer and a member of the Board of Directors. Transmeta develops and sells software-based microprocessors and related hardware and software technologies that enable computers to simultaneously offer long battery life, high performance and x86 compatibility. Transmeta's family of energy efficient Crusoe® microprocessors is targeted at the notebook and Internet appliance segments of the mobile Internet computer market, as well as ultra-dense servers and a range of embedded applications.

Before joining Transmeta, Perry held a series of management positions at Cirrus Logic, which he joined in December 1995. From April 1998 to April 2002, Perry served as Vice President and General Manager, during which period he managed, in succession, Cirrus' Embedded Processors Division, Crystal Products Division, and Optical Products Division. As Vice President and General Manager of the Crystal Products Division, Perry played an integral role in the development of the company's new consumer-focused digital entertainment vision. Also under Perry's leadership, Cirrus Logic developed the Maverick™ processor family, which quickly established worldwide leadership positions in the MP3 class of portable digital audio players.

Before joining Cirrus Logic, Perry held positions at Advanced Micro Devices where he served as Strategic Marketing Manager, and at Motorola as a Multimedia Systems and Applications Manager. Perry earlier served as an Assistant Professor of Electrical Engineering at Texas Tech University where he focused on signal and image processing research.

Perry serves on the Board of Directors for the Consumer Electronics Association, to which he was appointed in January 2002, and is widely recognized as an industry expert. In 2001, CNET declared that Perry "just might have as much influence on the shape of digital music as Napster's file-swapping service or any of the music studios." Perry also serves as a board member of the Austin Film Society.

He holds B.S., M.S. and Ph.D. degrees in Electrical Engineering from Oklahoma State University.

Panel Discussion and Luncheon
Wednesday, 12:15 pm – 1:45 pm
Greenwood Cultural Center

Paul Kolodzy, Chairman FCC Task Force on Spectrum Policy
The Future of Telecom

Paul Kolodzy, the newly named Chair of the FCC Task Force on Spectrum Policy, will chair a panel discussion on the "Future of Telecom". Panelists will consist of representatives of the telecom industry including some of the Chief Technology Officers of major telecom companies. Lunch will be served at 12:15 pm, and the panel discussion will begin shortly thereafter. Please join us for lunch and a stimulating discussion in the Greenwood Cultural Center. The Greenwood Cultural Center is located just behind Main Hall on the OSU-Tulsa campus.

Invited Presentations

RFID Implementation
Monday, August 5, 2:00-3:00 pm
OSU-Tulsa North Hall Room 260
Terry Alderson, *Boeing – Wichita Division*

Radio Frequency Identification (RFID) is an emerging technology that has had limited use in manufacturing environments. One of the premier aerospace companies discusses their journey through RFID. In this presentation they will share their journey with you, including an overview of the technology, initial findings, industry analysis, testing, pilots, business application, and the future use of RFID in their environment

The Serially Attached SCSI (SAS) Interface
Tuesday, August 6, 10:40-11:40am
OSU-Tulsa North Hall Room 260
John Worden, *Seagate Technology*

For more than 15 years, the Small Computer Systems Interface (SCSI) has been the mainstay enterprise storage rigid disc drive interface. In keeping with the computer industry's migration from bus architectures to switched serial interfaces, the new Serially Attached SCSI (SAS) interface extends the SCSI architecture into the future with higher interface performance, higher data integrity, and more flexible configurations. This presentation provides a technical overview of the SAS interface.

ONR / DoD Research Programs in Nanotechnology
Tuesday, August 6, 2:00-3:00 pm
OSU-Tulsa North Hall Room 260
Dr. Clifford Lau, *Office of Naval Research*

In January 2000 then President Clinton announced the National Nanotechnology Initiative to significantly increase the U.S. federal government's investments in nanotechnology. This initiative was the culmination of several years of planning by an interagency working group. Since then we have seen substantial increases in funding in the U.S. and all over the world. Nanotechnology has triggered the imagination of scientists and

engineers as the next industrial revolution. Nanotechnology is involved in many disciplines including physics, chemistry, materials, electronics, and others. The Navy/DoD nanotechnology research programs are focused on three areas of critical importance: nanomaterials by design, nanoelectronics including nanomagnetics and nanophotonics, and nanobiodevices. For DoD, nanotechnology offers the potential for enhanced capabilities in practically all areas of warfighting. In this presentation, Navy/DoD nanotechnology research programs and research opportunities in nanotechnology will be discussed.

Telecom Infrastructure Issues
Wednesday, August 7, 2:00-2:30 pm
OSU-Tulsa North Hall Room 260
Mathew Oommen, *Optical Datacom*

Mathew Oommen, Chief Technology Officer of Optical Datacom, will discuss several points concerning key telecommunications infrastructure issues that would address network challenges – enabling profitability of telecom companies in the future. This invited presentation will compliment the "Future of Telecom" panel discussion held at the Greenwood Cultural Center.

Exhibits

The 45th IEEE International Midwest Symposium exhibits will be open in Room 151 North Hall, from Monday, August 5th, through Wednesday, August 7th at Oklahoma State University-Tulsa. Exhibits will be open to attendees during the following hours:

Monday, August 5, 2002.....12:00 Noon - 5:00 pm
Tuesday, August 6, 2002 .....9:00 am - 6:00 pm
Wednesday, August 7, 2002 .....9:00 am - 5:00 pm

All booths will be open during show hours with a representative present to discuss products and services with symposium delegates. Morning and afternoon coffee breaks will be held near the exhibit hall.

IEEE MWSCAS Career Fair
Tuesday, August 6, 2002

In association with the 45th IEEE Midwest Symposium on Circuits and Systems, an **IEEE MWSCAS CAREER FAIR** is scheduled Tuesday, August 6, 2002. The Career Fair will be held from 1:00 pm – 5:00 pm in Main Hall on the OSU-Tulsa Campus.

Employers, graduate colleges, and faculty will attend this special Career Fair that will showcase advanced Electrical and Computer Engineering talent from throughout the United States and the World!

- Are you looking for Electrical Engineering "Graduate Students"?
- Are you looking for "Employees" with Electrical and/or Computer Engineering backgrounds?
- Are you looking for a "Faculty Member" in Electrical and/or Computer Engineering?

This Career Fair will not only promote represented companies on an international basis, but is also designed to provide you with opportunities for making contacts with many candidates – **the best-of-the-best in Electrical and Computer Engineering!**

Local Conference Transportation

Shuttle transportation between the Adam's Mark Hotel and OSU-Tulsa will be provided free of charge during the time the conference is in session. Shuttle buses are orange with an OSU logo on the side. A bus schedule will be posted at the Adam's Mark Hotel and at the OSU-Tulsa registration desk.

Sponsors of the 45th IEEE International Midwest Symposium on Circuits and Systems

We gratefully acknowledge the generous support of the following organizations and individuals that have sponsored this year's MWSCAS:

- **IEEE Circuits and Systems Society**
- **Oklahoma State University**
- **National Science Foundation**
- **Williams Communications Group**, Tulsa, OK
- **Center of Excellence in Information Technology and Telecommunications (COEITT)**, Tulsa, OK
- **Phillips Petroleum Company**, Bartlesville, OK
- **Halliburton Company**, Dallas, TX
- **Seagate Technology, LLC**, Oklahoma City, OK
- **Frontier Electronic Systems**, Stillwater, OK
- **Agilent Technologies**, Fort Collins, CO
- **Optical Datacom**, Tulsa, OK
- **FlightSafety International**, Tulsa, OK
- **Sciperio**, Stillwater, OK
- **Oklahoma Gas & Electric**, Oklahoma City, OK
- **Ericsson Inc**., Plano, TX
- **AFN Communications**, Tulsa, OK
- **Stillwater Designs - Kicker**, Stillwater, OK
- **Nomadics, Inc**., Stillwater, OK
- **AEP-Public Service Company of Oklahoma,** Tulsa, OK
- **Williams**, Tulsa, OK
- **Kay and Steve Wyatt**, Bartlesville, OK
- **McLeodUSA, Inc**., Tulsa, OK
- **WORLDCOM**, Tulsa, OK

MWSCAS 2002 Technical Schedule

Saturday August 3, 2002

6:00 pm – 8:00 pm	Registration – Adam's Mark Hotel Second Floor (near the hotel registration desk)

Sunday August 4, 2002

8:00 am – 2:30 pm	Registration – OSU-Tulsa North Hall First Floor
8:00 am – 6:00 pm	Email Room – OSU-Tulsa Main Hall First Floor Room 1308
10:00 am – 5:00 pm	IEEE Region 5 Chapters Meeting – OSU-Tulsa North Hall Room 106
9:00 am – 5:00 pm	Full-Day Tutorials – OSU-Tulsa North Hall Second Floor
2:00 pm – 5:00 pm	Half-Day Tutorials – OSU-Tulsa North Hall Second Floor
4:00 pm – 8:00 pm	Registration-- Adam's Mark Hotel Second Floor
6:00 pm – 8:00 pm	MWSCAS Welcome Reception – Adam's Mark Hotel Ballroom First Floor

Monday August 5, 2002

7:00 am – 5:00 pm	Registration – OSU-Tulsa North Hall First Floor
7:00 am – 6:00 pm	Email Room – OSU-Tulsa Main Hall First Floor Room 1308
8:00 am – 8:20 am	Opening Session: Welcome by OSU-Tulsa President Gary Trennepohl and Karl Reid, Dean of the College of Engineering Architecture and Technology – OSU-Tulsa Auditorium
8:20 am – 11:40 am	Student Paper Contest – OSU-Tulsa Auditorium, North Hall
12:15 pm – 1:45 pm	Awards Luncheon – Adam's Mark Hotel Ballroom First Floor
2:00 pm – 3:20 pm	Technical Sessions – OSU-Tulsa North Hall Second Floor
2:00 pm – 3:00 pm	Invited Presentation: RFID Implementation, Terry Alderson, Boeing – Wichita Division, OSU-Tulsa North Hall Room 260
3:20 pm – 3:40 pm	Afternoon Coffee Break – OSU-Tulsa North Hall Room 151
3:40 pm – 5:00 pm	Technical Sessions – OSU-Tulsa North Hall Second Floor
6:30 pm – 8:30 pm	IEEE MWSCAS Steering Committee Dinner and Meeting – Adam's Mark Hotel Promenade (Second Floor)

Tuesday August 6, 2002

7:00 am – 5:00 pm	Registration – OSU-Tulsa North Hall First Floor
7:00 am – 6:00 pm	Email Room – OSU-Tulsa Main Hall First Floor Room 1308
8:00 am – 9:00 am	Keynote Speech: Howard Janzen, CEO Williams Communications – "Telecom Market Place: A View from the Top", OSU-Tulsa Auditorium, North Hall

9:00 am – 10: 20 am	Technical Sessions – OSU-Tulsa North Hall Second Floor
10:20 am – 10:40 am	Morning Coffee Break – OSU-Tulsa North Hall Room 151
10:40 am – Noon	Technical Sessions – OSU-Tulsa North Hall Second Floor
10:40 am – 11:40 am	Invited Presentation: The Serially Attached SCSI (SAS) Interface, John Worden, Seagate Technology, OSU-Tulsa North Hall Room 260
Noon – 2:00 pm	IEEE North American Chapter Chair's Meeting – Adam's Mark Hotel Promenade (Second Floor)
1:00 pm – 5:00 pm	MWSCAS Career Fair – OSU-Tulsa Main Hall
2:00 pm – 3:20 pm	Technical Sessions – OSU-Tulsa North Hall Second Floor
2:00 pm – 3:00 pm	Invited Presentation: ONR / DoD Research Programs in Nanotechnology, Dr. Clifford Lau, Office of Naval Research, OSU-Tulsa North Hall Room 260
3:20 pm – 3:40 pm	Afternoon Coffee Break – OSU-Tulsa North Hall Room 151
3:40 pm – 5:00 pm	Technical Sessions – OSU-Tulsa North Hall Second Floor
5:30 pm – 11:30 pm	Discoveryland and the play *Oklahoma!* (Buses leave from Adam's Mark Hotel lower lobby in front of the Ballroom beginning promptly at 5:30 pm)

Wednesday August 7, 2002

7:00 am – 4:00 pm	Registration – OSU-Tulsa North Hall First Floor
7:00 am – 6:00 pm	Email Room – OSU-Tulsa Main Hall First Floor Room 1308
8:00 am – 9:00 am	Keynote Speech: Matthew Perry, CEO Transmeta – *Mobile Computing* OSU-Tulsa Auditorium, North Hall
9:00 am – 10: 20 am	Technical Sessions – OSU-Tulsa North Hall Second Floor
10:20 am – 10:40 am	Morning Coffee Break – OSU-Tulsa North Hall Room 151
10:40 am – Noon	Technical Sessions – OSU-Tulsa North Hall Second Floor
12:05 pm – 1:45 pm	Luncheon and Panel Discussion "The Future of Telecom", chaired by Paul Kolodzy – Greenwood Cultural Center (adjacent to the OSU-Tulsa campus)
2:00 pm – 3:20 pm	Technical Sessions – OSU-Tulsa North Hall Second Floor
2:00 pm – 2:30 pm	Invited Presentation: Telecom Infrastructure Issues, Mathew Oommen, Optical Datacom, OSU-Tulsa North Hall Room 260
3:20 pm – 3:40 pm	Afternoon Coffee Break – OSU-Tulsa North Hall Room 151
3:40 pm – 5:00 pm	Technical Sessions – OSU-Tulsa North Hall Second Floor

MWSCAS 2002 Social Events and Tours Schedule

Saturday August 3, 2002

6:00 pm – 8:00 pm	Registration – Adam's Mark Hotel Second Floor

Sunday August 4, 2002

8:00 am – 2:30 pm	Registration – OSU-Tulsa North Hall First Floor
1:00 pm – 6:00 pm	Oklahoma City National Memorial Tour – Leave from the lower lobby of Adam's Mark Hotel in front of the Ballroom
4:00 pm – 8:00 pm	Registration-- Adam's Mark Hotel Second Floor
6:00 pm – 8:00 pm	MWSCAS Welcome Reception – Adam's Mark Hotel Ballroom First Floor

Monday August 5, 2002

7:00 am – 5:00 pm	Registration – OSU-Tulsa North Hall First Floor
10:30 am – Noon	Tour of Williams Communications (Leave from Adam's Mark Hotel Second Floor near Hotel Registration Desk)
11:00 am – 2:30 pm	Utica Square and Lyon's Store Shopping Tour – Leave from Adam's Mark Hotel lower lobby in front of the Ballroom
12:15 pm – 1:45 pm	Awards Luncheon – Adam's Mark Hotel Ballroom First Floor
1:00 pm – 6:00 pm	Oklahoma City National Memorial Tour – Leave from Adam's Mark Hotel lower lobby in front of the Ballroom
2:00 pm – 3:30 pm	Tour of Williams Communications (Leave from Adam's Mark Hotel Second Floor near the Hotel Registration Desk)
3:30 am – 5:00 pm	Tour of Williams Communications (Leave from Adam's Mark Hotel Second Floor near the Hotel Registration Desk)
4:00 pm – 5:30 pm	Flight Safety International Tour – Leave from Adam's Mark Hotel lower lobby in front of the Ballroom
5:30 pm – 7:00 pm	Flight Safety International Tour – Leave from Adam's Mark Hotel lower lobby in front of the Ballroom

Tuesday August 6, 2002

7:00 am – 5:00 pm	Registration – OSU-Tulsa North Hall First Floor
10:00 am – 2:00 pm	Frankoma Pottery and Gilcrease Museum Tour – Leave from Adam's Mark Hotel lower lobby in front of the Ballroom
5:30 pm – 11:30 pm	Discoveryland and the play *Oklahoma!* (Buses leave from Adam's Mark Hotel lower lobby in front of the Ballroom beginning promptly at 5:30 pm)

Wednesday August 7, 2002

7:00 am – 4:00 pm	Registration – OSU-Tulsa North Hall First Floor
9:00 am – 5:00 pm	ABB Automation, Inc. and Woolaroc Museum Tour – Leave from Adam's Mark Hotel lower lobby in front of the Ballroom
11:00 am – 2:00 pm	Philbrook Art Museum Tour – Leave from Adam's Mark lower lobby in front of the Ballroom
12:05 pm – 1:45 pm	Luncheon and Panel Discussion "The Future of Telecom"– Greenwood Cultural Center (adjacent to the OSU-Tulsa campus)
1:00 pm – 6:00 pm	Oklahoma City National Memorial Tour – Leave from Adam's Mark Hotel lower lobby in front of the Ballroom
2:30 pm – 8:30 pm	OSU-Stillwater Tour and Eskimo Joe's – Leave from Adam's Mark Hotel lower lobby in front of the Ballroom

Welcome to Tulsa

What began as Tulsee Town in 1836 under a sturdy oak tree, which still stands at 18th and Cheyenne Streets, is today the second largest city in Oklahoma. Ask people to describe Tulsa, and you'll likely get many different answers. It was a city forever changed by the discovery of oil in 1901. It is home to art deco treasures and nationally renowned museums. Its African American heritage left its mark, in both the business and music worlds, and it's a city of nostalgia and special memories for countless Americans due to its location – on historic Route 66.

Whether you're here for business or pleasure, Tulsa is a cosmopolitan town that appeals to both young families and retirees. National touring exhibitions can be seen at the Philbrook Museum of Art, which was recently featured on the television program "America's Castles." For great western art, check out the Gilcrease Museum, and music legends are commemorated at Oklahoma's Jazz Hall of Fame. Other unique attractions worth a stop include the Elsing Museum, Ida Dennie Willis Museum of Miniatures, Dolls & Toys, Tulsa Air and Space Center and the Fenster Museum of Jewish Art

For a great shopping experience, a visit to Cherry Street or Utica Square is a must, and for those who would rather spend the afternoon on the links, Tulsa has several exclusive golf courses to choose from. During summer months, Rodgers and Hammerstein's classic musical, *Oklahoma!* is performed at the Discoveryland amphitheater where a barbecue dinner and roping lessons add to the evening's entertainment. Tulsa is also home to several outstanding events too numerous to list, but those worth a mention include Mayfest, the Gatesway International Balloon Festival, Oktoberfest and the Tulsa Powwow of Champions.

Useful Information

Electronic Mail Services: Electronic mail service will be provided at OSU-Tulsa Main Hall Room 1308 by the Master of Science and Telecommunication Management Program during the hours of 7:00 am-6:00 pm.

Tourist Information: (800) 558-3311 or www.VisitTulsa.com

Adam's Mark Hotel: 100 E. 2nd Street, Tulsa, Oklahoma 74103, (918) 582-9000

Area code for Tulsa: (918)

Main number for OSU-Tulsa Campus: (918) 594-8000.

Climate: Historical daily average highs and lows for the August 4-7 period are 93 degrees F and 71 degrees F, respectively.

Discoveryland and *Oklahoma!*

Designated The National Home of Rodgers and Hammerstein's *Oklahoma!* musical, this theatre production is presented annually each summer in a beautiful 2000 seat outdoor amphitheater complex by 50 of America's most talented performers -- complete with horses, wagons, and of course, a real surrey with a fringe on top! Grand ranch style dinner, Indian dancing, western gift shop, ice cream parlor, and children's activities top off the evening.

Tuesday August 6, 2002: Buses and Vans will provide transportation to Discoveryland. Buses will leave from the Adam's Mark Hotel lower lobby in front of the Ballroom at 5:30pm. Wear comfortable clothes and shoes, this is an outdoor attraction. Cattleman's ranch dinner will be served from 6:00pm to 7:30pm, Native American dancing at 7:00pm, a western musical review starts at 7:30pm and the play *Oklahoma!* starts at 8:00pm

Optional Tours

Several optional tours have been arranged for attendees of MWSCAS-2002 and their traveling companions. Pre-registration is advised because decisions to cancel low enrollment tours will be made 24 hours prior to the tour. Your money will be refunded in full if a low-enrollment tour is canceled. On-site registration will also be available on an "as available" basis at the tour desk in Room 150 North Hall at OSU-Tulsa.

FlightSafety International
Monday August 5, 2002, 4:00 pm – 5:30 pm, and 5:30 pm – 7:00 pm

The Simulation Systems Division (SSD) of FlightSafety International is responsible for the design, manufacture and support of the training devices required by FlightSafety. Additionally, SSD supplies training devices to FlightSafety, Boeing and other outside customers. These customers currently are predominately military. SSD designs and manufactures full flight simulators and flight training devices. These devices are designed to meet the most rigorous requirements of the FAA and other qualifying agencies worldwide.

The tour of SSD will include a briefing covering FSI's history, business operation, SSD's products and their development. The tour itself will approximately follow the design and manufacturing path a typical simulator will follow including; data acquisition, design, manufacturing, hardware/software integration, testing acceptance, shipping and qualification.

Oklahoma City National Memorial Center
Sunday, August 4, 1:00-6:00 pm, Monday, August 5, 1:00-6:00 pm, and Wednesday, August 7, 1:00-6:00 pm

The Memorial Center is an interactive learning museum that occupies the west end of the former Journal Record Building. Built in 1923, this building withstood the April 19, 1995, bombing and is listed on the National Register of Historic Places. The second component mandated by the Memorial's mission statement, the Memorial Center, will take you on a chronological, self-guided tour through the story of April 19, 1995 and the bombing of Oklahoma City's Alfred P. Murrah Federal Building. The cost of $25 per person includes the roundtrip coach to the site.

Lyon's Indian Store and Utica Square
Monday, August 5, 11:00 am – 3:00 pm

Lyon's Indian Store houses the largest selection of Indian goods and Oklahoma souvenirs in Tulsa. You will have an opportunity to shop for silver and turquoise Indian jewelry, moccasins, rugs, pottery and Indian art.

The second portion of the tour will be a stop at Utica Square. Have lunch on your own and then experience some of the best shopping that Tulsa has to offer. Stores include Saks Fifth Avenue, Ann

Taylor, Talbot's, Pottery Barn and Williams Sonoma. The cost of $5.00 per person includes transportation to both locations.

Frankoma Pottery Tour and Gilcrease Art Museum
Tuesday, August 6, 10:00 am – 2:00 pm
From the hand-created molds to the individual finishing, Frankoma's blend of old-world skills and modern production techniques yields the finest giftware and tableware available.

The Gilcrease Museum houses the world's largest, most comprehensive collection of art of the American West. In addition, Gilcrease offers an unparalleled collection of Native American art and artifacts, a hands-on, interactive exhibition highlighting the art, culture and history of Mexico, and a distinguished collection of historical manuscripts, documents, and maps. Have lunch on your own at the Rendezvous Restaurant at the Gilcrease Museum. The cost of $5.00 per person includes transportation to both locations.

Philbrook Museum of Art
Wednesday, August 7, 10:00 am – 1:00 pm
Philbrook is one of America's top sixty-five museums and one of only five museums with the unique combination of historic home, art gallery and gardens. Have lunch on your own at La Villa Restaurant at Philbrook. The cost of $10.00 person includes transportation and admission.

ABB Automation, Inc. and Woolaroc Museum
Wednesday, August 7, 9:00 am – 5:00 pm
ABB Automation, Inc. began in 1988 with the merger of two world leaders in power technology and automation: Asea (power technology) and BBC (hydroelectric power stations, controls, locomotion and data transmission). Their combined 120 years of technological and engineering achievements created one of the world's largest electrical engineering companies, Asea Brown Boveri Ltd. (ABB Inc). In 1989 ABB began to strategically acquire power transmission and power distribution businesses of Westinghouse Electric, global automation, and alternative energy. This tour will be in conjunction with a tour of Woolaroc Museum.

If there's one last undiscovered treasure left in the United States, it surely must be a place called Woolaroc. Hidden away in the rugged Osage Hills of Northeastern Oklahoma, in the heart of the U.S., Woolaroc is an anomaly. Located on 3600 acres, it is part Western art museum, part wildlife refuge, and part nature trail. It has the world's largest collection of colt firearms, and has a number of collections of cultural and historical importance. It was founded in 1925 as a private ranch for the oilman Frank Phillips and has continued to grow in scope and importance. From its 750 animals to its collection of more than 10,000 works of Native American and western art and artifacts, from the historic Frank Phillips lodge to its beautiful woods and lakes, Woolaroc is intriguing, individual and inviting.

Williams Communications
Monday August 5, 2002, 10:30 am – Noon, 2:00 pm – 3:30 pm, and 3:30 pm – 5:00 pm
Tour the Williams Communications Group new building located at One Technology Center, Tulsa Oklahoma next to the Adam's Mark Hotel. The 15-story 750,000 square foot vertically stacked technology tower covers one city block. Energy modeling indicates the building will use approximately 50% of the energy of comparable buildings thanks to the innovative Solar Well on the east side of the building. The building is designated with a 16' floor-to-floor dimension, which maximizes ceiling height. When completed, the new network operations center will be a two-story 160-station monitoring center for Williams Communications 40,000-mile network and video feeds. The 10th floor is dedicated to a conference center that will have 5 conference rooms and two large training rooms. The office floors were "modeled" after a University Campus and provide a variety of meeting places with opportunities to socialize to foster shared knowledge. Each floor contains an Internet café, a library, and a common conferencing area.

A Few Things to See and Do

Cinemark IMAX Theatre

918-307-2629, Adults $8.50 and children $6.50.
Oklahoma's first theatre of its kind, located in the Cinemark Megaplex at 71st and I-169 (Mingo Valley Expressway). The 5 stories tall by 7 stories wide screen provides images of unsurpassed size, clarity and impact, enhanced by a superb specially designed sound system. Both 2D and 3D IMAX films will play regularly at the theatre. A movie themed cafe serving appetizers, gourmet coffee, sandwiches and desserts is also on site, as well as a 16 screen movie cinema.

Creek Nation Tulsa Bingo

918-299-8515, http://www.tulsabingo.com
Come play at Tulsa's oldest and favorite place to win thousands! Play Rocket Bingo, the hottest sensation in fast-action high stakes progressive video bingo. Win thousands on the progressive four-ball jackpot played daily.

Greenwood Cultural Center

918-583-4545, 322 N. Greenwood Avenue (just behind OSU-Tulsa Main Hall)
Located in the historic Greenwood district, once known as the "Black Wall Street" of America. It is the location of the state's Jazz Hall of Fame with a computerized display that gives information about members and plays samples of their work. There is also a photographic exhibit of the tragic 1921 riot, music, books, memorabilia, and a gift shop.

Missions Memorial Museum and Gardens

918-459-0431, http://missionary.net/memorial
World class exhibits and spectacular stories of personal sacrifice are conveyed in this state-of-the-art museum. Attractions include a full-scale working replica of the Gutenberg press, the catacombs of Rome, an outstanding ancient Bible collection, rare art, and exhibits honoring the lives of courageous heroes of faith throughout history. Be inspired by the four-acre Memorial Gardens featuring one of Oklahoma's largest man-made waterfalls, walking paths connecting 20 stations of pictorial information intertwined through trees, ponds and foliage. A unique gift shop with snack bar completes your tour.

Tulsa Zoo and Living Museum

918-669-6600, http://www.TulsaZoo.org
The Tulsa Zoo, which is unique for combining animal exhibits with natural history museum exhibits, offers an exciting journey into the natural world where visitors can get nose to nose with a chimpanzee or a polar bear, and discover the secrets of the elephants through interactive displays. The Tulsa Zoo is set within 70 beautiful acres, and is home to more than 1,400 animals, many of which are rare and endangered. A handicapped accessible train gives visitors a tour around the zoo. Two gift shops, a full service restaurant, and plenty of snack bars will round out any visit.

Technical Program Schedule and Abstracts

Session codes break down as follows:

First Character: **Day of Session**	Second, Third & Fourth Characters: **Session Time**	Fifth Character: **Session Type**	Sixth, Seventh & Eighth Characters **Room Number**
M = Monday **T** = Tuesday **W** = Wednesday	**AM1** = 9:00 – 10:20 **AM2** = 10:40 – 12:00 **PM1 =** 2:00 – 3:20 **PM2** = 3:40 – 5:00	**P** = Poster **L** = Lecture	**AUD** = Auditorium

Example: MPM2P-140

Day: Monday, **Time:** 3:40 pm, **Type:** Poster**, Room:** 140

Time	Auditorium	Room 140 - Posters	Room 151	Room 260
Monday **August 05, 2002** **8:00am-12:00pm**	MAM0L-AUD **Student Paper Contest** *Chair: Rick Branner*			
Monday **August 05, 2002** **2:00pm-3:20pm**		MPM1P-140 **Sensors, Analog Filters, Data Conversion** *Chair: Sherif Michael*	**EXHIBITS** ***Monday*** ***2:00pm-5:00pm***	***2:00pm - 3:00pm*** **INVITED TALK:** **RFID Implementation** **Terry Alderson,** ***Boeing – Wichita Div.***
BREAK			***BREAK ROOM***	
Monday **August 05, 2002** **3:40pm-5:00pm**		MPM2P-140 **Mixed Signal VLSI** *Chair: Igor Filanovsky*	**EXHIBITS** ***Monday*** ***2:00pm-5:00pm***	
Tuesday **August 06, 2002** **8:00am-9:00am**	***KEYNOTE SPEAKER:*** **Howard E. Janzen,** President & CEO Williams Communications **Telecom Market Place: A View from the Top**			
Tuesday **August 06, 2002** **9:00am-10:20am**		TAM1P-140 **High Performance Digital Circuits and VLSI Design Methodologies** *Chair: Cristian Chitu*	**EXHIBITS** ***Tuesday*** ***9:00am-5:00pm***	
BREAK			***BREAK ROOM***	
Tuesday **August 06, 2002** **10:40am-12:00pm**		TAM2P-140 **VLSI Systems** *Chair: TBD TBD*	**EXHIBITS** ***Tuesday*** ***9:00am-5:00pm***	***10:40am - 11:40pm*** **INVITED TALK:** **The Serially Attached SCSI (SAS) Interface** **John Worden,** ***Seagate Technology***
Tuesday **August 06, 2002** **2:00pm-3:20pm**		TPM1P-140 **DSP System Design and Implementation** *Chair: Mohamad Farooq*	**EXHIBITS** ***Tuesday*** ***9:00am-5:00pm***	***2:00pm - 3:00pm*** **INVITED TALK:** **ONR / DoD Research Programs in Nanotechnology** **Dr. Clifford Lau,** ***Office of Naval Research***
BREAK			***BREAK ROOM***	
Tuesday **August 06, 2002** **3:40pm-5:00pm**		TPM2P-140 **Signal Processing** *Chair: Tran Thong*	**EXHIBITS** ***Tuesday*** ***9:00am-5:00pm***	
Wednesday **August 07, 2002** **8:00am-9:00am**	***KEYNOTE SPEAKER:*** **Matthew R. Perry** President & CEO Transmeta Corporation **Mobile Computing**			
Wednesday **August 07, 2002** **9:00am-10:20am**		WAM1P-140 **Communications Systems** *Chair: Edward Daniel*	**EXHIBITS** ***Wednesday*** ***9:00am-12:00pm***	
BREAK			***BREAK ROOM***	
Wednesday **August 07, 2002** **10:40am-12:00pm**		WAM2P-140 **Neural Networks** *Chair: Roger Schultz*	**EXHIBITS** ***Wednesday*** ***9:00am-12:00pm***	
Wednesday **August 07, 2002** **2:00pm-3:20pm**		WPM1P-140 **Signal Image Analysis and Speech Processing** *Chair: Mary Kohler*		***2:00pm - 2:30pm*** **INVITED TALK: Telecom Infrastructure Issues** **Mathew Oommen, *Optical Datacom***
BREAK			***BREAK ROOM***	
Wednesday **August 07, 2002** **3:40pm-5:00pm**		WPM2P-140 **Microwave & Optical Systems and Synthesizers** *Chair: Chia-Ming Lu*		

Time	Room 209	Room 211	Room 213	Room 214	Room 216
Monday August 05, 2002 8:00am-12:00pm					
Monday August 05, 2002 2:00pm-3:20pm	MPM1L-209 **Amplifiers I** *Chair: Mark Schlarmann*	MPM1L-211 **RF & Microwave Oscillators I** *Chair: Yumin Zhang*	MPM1L-213 **Oversampled Data Conversion I** *Chair: TBD TBD*	MPM1L-214 **VLSI Power, Noise and Simulation I** *Chair: Peter-Michael Seidel*	MPM1L-216 **VLSI Testing I** *Chair: Mona Zaghloul*
BREAK					
Monday August 05, 2002 3:40pm-5:00pm	MPM2L-209 **Amplifiers II** *Chair: Mark Schlarmann*	MPM2L-211 **RF & Microwave Oscillators II** *Chair: Yumin Zhang*	MPM2L-213 **Oversampled Data Conversion II** *Chair: Kwong Chao*	MPM2L-214 **VLSI Power, Noise and Simulation II** *Chair: Peter-Michael Seidel*	MPM2L-216 **VLSI Testing II** *Chair: Mona Zaghloul*
Tuesday August 06, 2002 8:00am-9:00am					
Tuesday August 06, 2002 9:00am-10:20am	TAM1L-209 **Amplifiers III** *Chair: Mohamad Sawan*	TAM1L-211 **RF & Microwave Oscillators III** *Chair: Jose Silva-Martinez*	TAM1L-213 **Nyquist Rate Data Conversion I** *Chair: Won Namgoong*	TAM1L-214 **IP, Embedded Cores and Systems on a Chip I** *Chair: Wael Badawy*	TAM1L-216 **VLSI Routing, Partitioning and Placement I** *Chair: Robert Reese*
BREAK					
Tuesday August 06, 2002 10:40am-12:00pm	TAM2L-209 **Current Amplifiers** *Chair: Mohamad Sawan*	TAM2L-211 **RF and Microwave Filters** *Chair: Jose Silva-Martinez*	TAM2L-213 **Nyquist Rate Data Conversion II** *Chair: Won Namgoong*	TAM2L-214 **IP, Embedded Cores and Systems on a Chip II** *Chair: Wael Badawy*	TAM2L-216 **VLSI Routing, Partitioning and Placement II** *Chair: Robert Reese*
Tuesday August 06, 2002 2:00pm-3:20pm	TPM1L-209 **Sensor Electronics** *Chair: Franco Maloberti*	TPM1L-211 **RF & Microwave Amplifiers and Mixers I** *Chair: Danny Pinckley*	TPM1L-213 **Testing and BIST I** *Chair: Degang Chen*	TPM1L-214 **Low Power Circuits and Architecture I** *Chair: Lex Akers*	TPM1L-216 **VLSI Synthesis I** *Chair: Mitch Thornton*
BREAK					
Tuesday August 06, 2002 3:40pm-5:00pm	TPM2L-209 **Image Sensors** *Chair: Franco Maloberti*	TPM2L-211 **RF & Microwave Amplifiers and Mixers II** *Chair: Danny Pinckley*	TPM2L-213 **Testing and BIST II** *Chair: Degang Chen*	TPM2L-214 **Low Power Circuits and Architecture II** *Chair: Lex Akers*	TPM2L-216 **VLSI Synthesis II** *Chair: Mitch Thornton*
Wednesday August 07, 2002 8:00am-9:00am					
Wednesday August 07, 2002 9:00am-10:20am	WAM1L-209 **Analog Filters I** *Chair: Jin Liu*	WAM1L-211 **Microwave Devices and Materials** *Chair: James West*	WAM1L-213 **Optical Circuits and Systems I** *Chair: Sherif Michael*	WAM1L-214 **Novel Circuits & Architecture** *Chair: Michael Weeks*	WAM1L-216 **VLSI and Programmable Logic Applications I** *Chair: Jeffrey Coleman*
BREAK					
Wednesday August 07, 2002 10:40am-12:00pm	WAM2L-209 **Analog Filters II** *Chair: Jin Liu*	WAM2L-211 **Passive RF and Microwave Systems** *Chair: James West*	WAM2L-213 **Optical Circuits and Systems II** *Chair: Sherif Michael*	WAM2L-214 **Third and Fourth Generation Wireless Systems** *Chair: Annamalai Annamalai*	WAM2L-216 **VLSI and Programmable Logic Applications II** *Chair: Jeffrey Coleman*
Wednesday August 07, 2002 2:00pm-3:20pm	WPM1L-209 **Analog Filters III** *Chair: TBD TBD*	WPM1L-211 **Dividers/Doublers and Prescalers** *Chair: Rick Branner*	WPM1L-213 **Clock & Data Recovery Building Blocks** *Chair: J. Silva-Martinez*	WPM1L-214 **Software Radio** *Chair: K. Srikanteswara*	WPM1L-216 **VLSI Systems, Design and Simulation** *Chair: K. Thulasiraman*
BREAK					
Wednesday August 07, 2002 3:40pm-5:00pm	WPM2L-209 **Analog Filters IV** *Chair: TBD TBD*	WPM2L-211 **References** *Chair: Rick Branner*	WPM2L-213 **Communication System Performance Analysis** *Chair: Bon-Jin Ku*	WPM2L-214 **Ultra-wideband Radio** *Chair: Mike Buehrer*	WPM2L-216 **VLSI Design for Applications** *Chair: K. Thulasiraman*

Time	Room 218	Room 219	Room 221	Room 223	Room 225
Monday August 05, 2002 8:00am-12:00pm					
Monday August 05, 2002 2:00pm-3:20pm	MPM1L-218 **Wireless Networks I** *Chair: John Metzner*	MPM1L-219 **Neural Networks with Nonlinear Dynamics I** *Chair: Damon Miller*	MPM1L-221 **Analog Signal Processing** *Chair: Paul Hasler*	MPM1L-223 **Biomedical Signal and Image Processing I** *Chair: Marios Pattichis*	MPM1L-225 **Coding for Communications** *Chair: Monique Fargues*
BREAK					
Monday August 05, 2002 3:40pm-5:00pm	MPM2L-218 **Wireless Networks II** *Chair: John Metzner*	MPM2L-219 **Neural Networks with Nonlinear Dynamics II** *Chair: Damon Miller*	MPM2L-221 **DSP in Communications** *Chair: Paul Hasler*	MPM2L-223 **Biomedical Signal and Image Processing II** *Chair: Marios Pattichis*	MPM2L-225 **Non-stationary Signal Processing** *Chair: Monique Fargues*
Tuesday August 06, 2002 8:00am-9:00am					
Tuesday August 06, 2002 9:00am-10:20am	TAM1L-218 **Ad Hoc Networks** *Chair: Mingyan Liu*	TAM1L-219 **Neural Networks for Filtering and Instrumentation** *Chair: Roger Schultz*	TAM1L-221 **Special Purpose Filter Designs** *Chair: Domenic Ho*	TAM1L-223 **Multimedia and Content Based Retrieval** *Chair: Dipti Mukherjee*	TAM1L-225 **Power Systems I** *Chair: Philip Yoon*
BREAK					
Tuesday August 06, 2002 10:40am-12:00pm	TAM2L-218 **Networking Circuits and Systems** *Chair: Mingyan Liu*	TAM2L-219 **Aerospace Applications of Modeling, Control and Neural Networks** *Chair: Mark Motter*	TAM2L-221 **Detection and Enhancement** *Chair: Domenic Ho*	TAM2L-223 **Image and Video Coding** *Chair: Edward Delp*	TAM2L-225 **Power Systems II** *Chair: Philip Yoon*
Tuesday August 06, 2002 2:00pm-3:20pm	TPM1L-218 **Advanced Networking Systems I** *Chair: Bon-Jin Ku*	TPM1L-219 **Applications of Adaptive Systems I** *Chair: Edward Wilson*	TPM1L-221 **Mixed Signal & Signal Conversion Processing I** *Chair: J. Bruce*	TPM1L-223 **Signal and Image Analysis I** *Chair: Joe Havlicek*	TPM1L-225 **Power Electronics I** *Chair: Kaveh Ashenayi*
BREAK					
Tuesday August 06, 2002 3:40pm-5:00pm	TPM2L-218 **Advanced Networking Systems II** *Chair: Bon-Jin Ku*	TPM2L-219 **Applications of Adaptive Systems II** *Chair: Edward Wilson*	TPM2L-221 **Mixed Signal & Signal Conversion Processing II** *Chair: J. Bruce*	TPM2L-223 **Signal and Image Analysis II** *Chair: Joe Havlicek*	TPM2L-225 **Power Electronics II** *Chair: Kaveh Ashenayi*
Wednesday August 07, 2002 8:00am-9:00am					
Wednesday August 07, 2002 9:00am-10:20am	WAM1L-218 **Adaptive Methods in Wireless Communication Systems I** *Chair: Robert Soni*	WAM1L-219 **Neuro Control** *Chair: Mohammad Menhaj*	WAM1L-221 **Adaptive Signal and Image Processing I** *Chair: Guoliang Fan*	WAM1L-223 **Speech Processing and Analysis** *Chair: Mary Kohler*	WAM1L-225 **MPLS, MPLambdaS, and GMPLS Networks I** *Chair: Harleen Chhabra*
BREAK					
Wednesday August 07, 2002 10:40am-12:00pm	WAM2L-218 **Adaptive Methods in Wireless Communication Systems II** *Chair: Robert Soni*	WAM2L-219 **Programmable Logic Circuits** *Chair: Monte Tull*	WAM2L-221 **Adaptive Signal and Image Processing II** *Chair: Guoliang Fan*	WAM2L-223 **Watermarking and Coding** *Chair: Edward Delp*	WAM2L-225 **MPLS, MPLambdaS, and GMPLS Networks II** *Chair: Harleen Chhabra*
Wednesday August 07, 2002 2:00pm-3:20pm	WPM1L-218 **High Data Rate Modulation and Coding Techniques I** *Chair: Matt Valenti*	WPM1L-219 **High Performance Arithmetic Circuits Architectures I** *Chair: Mohamad Farooq*	WPM1L-221 **Adaptive IIR Filtering** *Chair: Neeraj Magotra*	WPM1L-223 **Low Sensitivity Digital Filter Designs** *Chair: Domenic Ho*	WPM1L-225 **Network Security I** *Chair: Raymond Garcia*
BREAK					
Wednesday August 07, 2002 3:40pm-5:00pm	WPM2L-218 **High Data Rate Modulation and Coding Techniques II** *Chair: Matt Valenti*	WPM2L-219 **High Performance Arithmetic Circuits Architectures II** *Chair: Mohamad Farooq*	WPM2L-221 **Adaptive Signal Processing Applications** *Chair: Victor DeBrunner*	WPM2L-223 **Multidimensional Filter Designs** *Chair: Domenic Ho*	WPM2L-225 **Network Security II** *Chair: Raymond Garcia*

MAM0L-AUD -- Student Paper Contest
Monday: 8:00 am – 12:00 pm
Chair: Rick Branner
University of California Davis

MAM0L-AUD -- High-Performance All-Digital Quadrature Frequency Synthesizer/ Mixer
Zhangwen Tang and Hao Min, *Fudan University*

In this paper, a high-performance all-digital quadrature frequency synthesizer/mixer applied to QAM modulation and demodulation is presented, which synthesizes 12-bit sine and cosine waveforms with a spectral purity of ¨C83.0dB. Also, it is capable of frequency, phase and quadrature amplitude modulation. An efficient look-up table method for calculating the sine/cosine function is employed, and a compressed algorithm that only calculates 1/8 sine function is proposed to reduce the volume of ROM. By taking advantage of sine and cosine symmetries, the size of the look-up table ROM is only 1/51 of that of traditional one.

MAM0L-AUD -- Nonlinear Analysis of CMOS LC-Tuned VCO Phase Noise
Sebastian Magierowski and Stefan Zukotynski, *University of Toronto*

A second order nonlinear stochastic differential equation is used as a tool for phase noise and jitter analysis in sub-micron CMOS LC VCOs. The negative resistance topology typical of integrated microwave designs is considered. Expressions for the phase noise characteristics are derived in terms of circuit parameters and shown to closely match simulation results. The insight gained is used to explore circuit design trade-offs.

MAM0L-AUD -- A 0.8V Ultra-low Power CMOS Operational Amplifier Design
Chuang Zhang, Ashok Srivastava, and Pratul Ajmera, *Louisiana State University*

In this paper, a low-power (±0.4V) operational amplifier is designed in a standard CMOS process. The amplifier has a dc gain 7000, and bandwidth 30 KHz. This design is done by combination of low voltage current mirror and forward biased between source and substrate of the MOSFET to reduce the threshold voltage.

MAM0L-AUD -- A Novel System for Measurement of Power System Parameters and Signals
Masoud Karimi-Ghartemani and Reza Iravani, *University of Toronto*

This paper presents various applications of a nonlinear adaptive notch filter which operates based on the concept of an enhanced phase-locked loop (PLL). Applications of the filter for on-line signal analysis for power systems protection, control and power quality enhancement are presented. The proposed scheme can be applied for signal analysis both under stationary and nonstationary conditions. Based on digital time-domain simulations, applications of the filter for (a) sinusoidal waveform peak detection, (b) frequency estimation, (c) harmonic identification/detection, (d) detection/extraction of individual components of a signal, (e) disturbance detection, (f) noise reduction in zero-crossings detection, and (g) amplitude (phase) demodulation for flicker estimation, are presented.

MAM0L-AUD -- RF Circuit Performance Degradation Due to Hot Carrier Effect and Soft Breakdown
Enjun Xiao and Jiann S. Yuan, *University of Central Florida*

A methodology to systematically study hot carrier and soft breakdown effects on RF circuits is proposed, and verified with a 2.45GHz low noise amplifier (LNA) and a 1GHz voltage controlled oscillator (VCO). MOSFETs of 0.16 µm technology are stressed, and DC and RF parameters are extracted and used for BTABERT and SpectreRF simulations to give RF circuit performance degradations due to HC and SBD effects with respect to operation time. Design guidelines for more reliable RF circuits are given after simulation and analysis.

MAM0L-AUD -- An Adaptive Low Power Texture Mapping Architecture for 3D Graphics

Jeevan Chittamuru and Wayne Burleson, *University of Massachusetts*

The migration of 3D graphics onto portable devices requires an increased emphasis on the development of low-power 3D graphic architectures. The texture mapping stage is one of the most power consuming stages of the 3D graphics pipeline, due to its extensive computations and off-chip memory accesses. In this paper an adaptive texture mapping architecture is proposed which mainly achieves low power by the application of data-pattern sensitive transformations to reduce the complexity of computations. These techniques have been shown to achieve power savings in the range of 30% to 53% from the interpolation unit, a main component of the texture mapping system. Two more techniques namely adaptive datapath partitioning and dynamic voltage scaling based on the algorithm selected for texture mapping are proposed for achieving significant power savings.

MAM0L-AUD -- Micro-Electromechanical Variable Capacitors for RF Applications

Mourad El-Gamal and Tommy Tsang, *McGill University*

This paper presents the principle of operation and design equations of MEMS-based variable capacitors designed using the MUMPs technology. Two prototypes with different tuning characteristics are examined. Measurements have shown that a tuning range of more than 35% is achievable at 2.4 GHz, with a self-resonant frequency of 4 GHz, and a maximum quality factor of 15. An analysis of the performance obtained is discussed, in the context of the characteristics of the fabrication process used.

MAM0L-AUD -- A Strategy for Reducing Clock Noise in Mixed-Signal Circuits

Erik Backenius, Mark Vesterbacka, and Robert Hägglund, *Linkoping University*

Digital switching noise is of major concern in mixed-signal circuits due to the coupling of the noise via a shared substrate to sensitive analog circuits. A significant noise source is the digital clock network that generally has a high switching activity. It is particularly difficult to dampen the high frequency components of the noise. In this work, we present a strategy that targets these problems. The approach is to generate a clock with smooth edges, i.e. reducing the high frequency components, and use a special digital flip-flop circuit that operates well with this clock.

MAM0L-AUD -- A 13W Current Mode Class D High Efficiency 1 GHz Power Amplifier

Anthony Long, Jingshi Yao, and Stephen Long, *University of California Santa Barbara*

13 watt Current Mode Class-D (CMCD) with 60% efficiency is presented. This amplifier is the highest power switch mode microwave power amplifier reported to date. The CMCD architecture is an improvement over the Voltage Mode Class-D in that the parasitic reactance in the active device can be absorbed into the tank circuit resulting in a zero voltage switching condition.

MAM0L-AUD -- Simple Adaptive Hetrodyne Filter

Biju Mullul Veedu and Michael Soderstrand *Oklahoma State University*

The tuning of the band pass filter in the simple heterodyne filter structure [1] can be done over a range of 90-degrees by changing the heterodyne frequency. However in this, the heterodyne frequency is constant and can be made adaptive by introducing a Digital Voltage Controlled Oscillator. The proposed design structure uses the Voltage Controlled Oscillator output that can be used as the heterodyne frequency so as to tune the band pass filter effectively.

MPM1L-209 -- Amplifiers I
Monday: 2:00 pm – 3:20 pm
Chair: Mark Schlarmann
Iowa State University

MPM1L-209 -- A Simple Way to Extend the Common-Mode Input-Voltage Range of the MOS Differential Pair

Bradley Minch, *Cornell University*

In this paper, we describe a simple technique involving indirect negative feedback that extends the useable common-mode input-voltage range of the MOS differential pair by a saturation voltage. In this method, we use a replica differential pair to sense when the bias transistor supplying the tail current falls out of saturation. We then set the bias voltage so that the sum of the two differential-pair output currents is equal to the bias current. We present experimental results from a version of the differential pair that was fabricated in a 0.5-um CMOS process along with a comparison with an identical differential pair with a fixed bias with respect to their common-mode input ranges.

MPM1L-209 -- Equivalent Gain Analysis for Nonlinear Operational Amplifiers

Chengming He, Le Jin, Hanjun Jiang, Degang Chen, and Randall Geiger, *Iowa State University*

For low-voltage, low-power circuit design, the linear model for operational amplifiers isn't able to accurately predict the static and the dynamic behavior of the circuit as it used to do. This paper introduces a nonlinear model for operational amplifiers based on the DC transfer characteristic. By using this nonlinear model, the behavior of an operational amplifier with feedback network can be described precisely. Equivalent open-loop gains of the operational amplifier for some typical purposes are studied in this paper. These equivalent gains can help identify the nonlinearities in the close-loop amplifier and determine the performance of the circuit.

MPM1L-209 -- A Wide Swing 1.5V Full Differential OP-AMP Using A Rail-to-Rail Analog CMFB Circuit

Hassan Maarefi, and Ali Parsa, *KavoshCom*, Hamid Hatamkhani, *UCLA*, and Darush Shiri, *Kavoshcom*

Design and simulation results of a CMOS fully differential op amp using continuous time rail-to-rail CMFB are presented. In the conventional source follower CMFB circuits because of substantial level shift due to VGS of source follower, outputs are restricted to have severed limited swing. In this paper two NMOS and PMOS CMFB are composed as complementary CMFBs to allow free output swing. The circuit is then simulated in 0.13ìm CMOS technology and performance parameters, which have been obtained, are much better than conventional methods. 2.4v Peak-to-Peak swing with a CMRR of118dB,are the simulated results.

MPM1L-209 -- A Highly Linear CMOS Amplifier For Variable Gain Amplifier Applications

Yonghui Tang, and Randall Geiger, *Iowa State University*

This paper reports the design of a highly-linear CMOS amplifier for Variable Gain Amplifier (VGA) applications. A better than 60dB 3rd harmonic distortion at differential output level of 1V peak-to-peak is obtained by utilizing a linearization scheme that does not rely on the active devices. The amplifier maintains 3dB bandwidth over 300MHz. A noise figure at 8.6dB is obtained with source impedance of 200 ohms. It is implemented in standard CMOS 0.25u process and consumes 40mA current under 3.3V power supply.

MPM1L-211 -- RF and Microwave Oscillators I
Monday: 2:00 pm – 3:20 pm
Chair: Yumin Zhang
Oklahoma State University

MPM1L-211 -- A Simple CMOS VCO
Srinivasan Venkatara and Yumin Zhang, *Oklahoma State University*

A simple CMOS ring oscillator is proposed as a novel VCO, where the frequency of the oscillator is controlled by the body voltage. An implementation with five inverters is simulated with Cadence, and the range of the oscillation frequency is found to be 271-289 MHz. The rate of frequency shift is verified by theoretical analysis.

MPM1L-211 -- An NMOS Inductive Loading Technique for Extended Operating Frequency CMOS Ring Oscillators
Apisak Worapishet, *Mahanakorn University of Technology,* and Manop Thamsirianunt, *National Electronics and Computer Technology Center*

The circuit architecture of the active inductive load based upon an nMOS transistor for frequency enhancement in CMOS ring oscillators is described. Emphasis is given to the performance analysis and design guidelines of the inductive loading technique as well as its theoretical comparison with the ordinary resistive loading ring oscillator. Implemented using a 0.35um, 3.3V CMOS process with fT=10GHz, the simulated 3-stage nMOS inductive ring oscillator meet the specified target at 2.4GHz even at slow process extreme and 125C temperature while consuming less than 52mW of power.

MPM1L-211 -- Design of a Colpitts Oscillator Using Micro-Strip-Line Inductor Compensed For Low Q
Chao Su, Streenath Thoka, Kee-Chee Tiew, and Randall Geiger, *Iowa State University*

In this paper, a modified differential bipolar Colpitts Voltage Controlled Oscillator (VCO) is presented. The VCO has a simulated tuning range of 25.45% centered at 45GHz. The on-chip inductor is implemented with microstrip lines, which have an inductance of 590pH at 45GHz and a Q of 1.4. To compensate for the low Q of the inductor, the Colpitts VCO is modified to include negative resistances (-Gm). The VCO operates from 3.3v supply. The power dissipation is 66mW at 45GHz. The VCO is implemented in a 120GHz fT SiGe BiCMOS process.

MPM1L-211 -- Distortionless RF Pulse Width Modulation
Poojan Wagh, Pallab Midya, and, Patrick Rakers, *Motorola Labs*

A method is presented to synthesize a switching signal which linearly encodes a complex-modulated RF signal to an RF carrier frequency. The switching distortion associated with this method is limited to high-pass components out of band. Consequently, the switching signal may be filtered after high efficiency amplification to produce the linear RF modulation. The method requires a switching frequency slightly higher than the highest frequency in the band of interest.

MPM1L-213 -- Oversampled Data Conversion I
Monday: 2:00 pm – 3:20 pm
Chair: TBA

MPM1L-213 -- Implementation of 1.5 V Low Power Two-path Decimation Filters for Communications Delta-Sigma Converters

Chia-Ming Liu and Chris Hutchens, *Oklahoma State University*

This paper reports on the fabrication of a low power decimation filter with a Two-path architecture [1]. The filter reduces the power consumption by better than 50% over previous work [2]-[5]. Instead of decimating data after filtering, the reported technique takes advantage of binary coefficients and performs data division before filtering. Based on the Two-path architecture, the adder clock rate as well as the number of additions is reduced. As a result, overall power efficiency is increased by a factor of better than two. Power is further reduced by implementing the design on Silicon-On-Sapphire (SOS) process with the reduction of drain-to-body capacitors. The presented Two-path filter has greater attenuation and a narrower transition band than an equivalent implementation of a Sinc filter although with somewhat greater complexity. The selected approach of FIR architecture with its linear phase and excellent delay power product is well suited for communications Delta-Sigma ADCs. The 64 times decimation filter was implemented in Peregrine SOS with a 4-bit input and an 18-bit output data width. The filter was functionally tested and operational up to 23MHz or 0.36Msps with a power dissipation of 8.3nW/Hz. Powered at 1.5V and operating at 10Msps, the filter consumes 1.5uW at standby and 85mW at operation.

MPM1L-213 -- A Fourth-Order Cascaded Sigma-Delta Modulator With DAC Error Cancellation Technique

Chun-Hsien Su and Kwong Chao, *Texas Tech University*

An architecture that improves the performance degradation caused by DAC nonlinearity in a cascaded multi-bit sigma-delta modulator is presented. The proposed architecture, with an extra feedback path in each internal stage, can totally cancel out the errors caused by DAC nonlinearity at the final stage and, in general, increases the shaping function of DAC errors by one order for the other internal stages as compared to the MASH structure. Behavioral simulation shows that the proposed fourth-order modulator has excellent immunity to DAC nonlinearity over the MASH structure when OSR is greater than 16. With maximum DAC differential nonlinearity of ±0.05LSB and an OSR of 64, an improvement of 20dB over the MASH structure has been observed.

MPM1L-213 -- Advantages of High-Pass Delta Sigma Modulators in Interleaved Delta Sigma Analog to Digital Converter

Tam Nguyen, Patrick Loumeau and Jean-Francois Naviner, *ENST*

Delta sigma modulators are widely used for low to moderate rate analog-to-digital conversions. But they are not adapted to high rate conversion because of the time over-sampling requirement. The use of parallel architecture is one of solutions to increase the frequency range of delta sigma ADCs. In this paper, we propose using high-pass delta sigma modulators in time-interleaved delta sigma ADC. The use of high-pass delta sigma modulators not only retains the performance of the converter but also eliminates the low frequency noises. It allows then to use simple adaptive channel gain equalization schemes to minimize the effects of the channel gain mismatches. Such an architecture can be obtained without adding much hardware complexities. In consequence, the architecture offers the potential of integrating high-precision, high-speed ADC together with digital signal processing functions using VLSI processes optimized for digital circuitry.

MPM1L-213 -- A 1.8V Continuous-Time Delta-Sigma Modulator with 2.5MHz bandwidth

Yi Zhang and Adrian Leuciuc, *State University of New York at Stony Brook*

This paper describes the implementation of a low-voltage, wide bandwidth, continuous-time low-pass Delta-Sigma modulator. The presented modulator operates at a supply voltage of 1.8V and can achieve a maximum SNDR of 74dB (more than 12 bits) for an oversampling ratio of 32 and in a bandwidth of 2.5 MHz.

MPM1L-214 -- VLSI: Power, Noise, and Simulation I
Monday: 2:00 pm – 3:20 pm
Chair: Peter-Michael Seidel
Southern Methodist University

MPM1L-214 -- RTL Power Modeling and Estimation Based on Bit and Word Level Switching Properties

Michael Eiermann and Walter Stechele, *Technical University of Munich*

We introduce the concept of a fast power estimation flow, based on RTL power macromodeling. It provides the capability to estimate power for complete processing steps of an algorithm using real data and considering the target hardware. For that, we developed efficient power modeling techniques based only on word and bit level switching information. The average errors achieved for several test modules and input stimuli are about 5%. Solutions for handling the complexity and ensuring the estimation accuracy are provided. The flow enables a speed up of about 100 times compared to gate level estimation, however having the same accuracy.

MPM1L-214 -- SDV2: Dynamic Visualization of VERILOG Simulations

Ralph Marczynski and Peter-Michael Seidel, *Southern Methodist University*

We are giving an introduction to SDV2 (SMU Dynamic Verilog Visualization), a software tool for dynamic visualization of Verilog simulations currently developed at SMU. Conventional Verilog simulations focus on computing and displaying waveforms for selected signal values over time. The SDV2 tool additionally allows to schematically visualize the module structure of a system described in Verilog and to animate signal propagations between module interfaces as dynamic transitions in the schematics. The dynamic visualization enhances conventional debugging of systems developed in Verilog hardware description language and simplifies the understanding of their dynamic behavior, which is useful both in educational and in industrial settings. In this paper we are describing the basic functionality of the SDV2 tool and we give some insight regarding the implementation structure.

MPM1L-214 -- Crosstalk Minimization For Multiple Clock Tree Routing

Ming-Fu Hsiao, and Malgorzata Marek-Sadowska, *University of California, Santa Barbara,* and Sao-Jie Chen, *National Taiwan University*

Crosstalk noise has been identified as a very important factor for deep submicron chip design. Signals running in parallel on the same layer can experience crosstalk noise. Among all the possible crosstalk noise sources, clock is the most important aggressor as well as victim. Besides, for modern chip design, there are usually more than one clock source, sometimes tens of clock sources. It is important to design the clock topologies for all the clocks running on the same chip to prevent possible crosstalk noise among them. In this paper, we deal with the minimization of inter-clock crosstalk. We propose algorithms to generate clock topology and routing to minimize effective crosstalk. The experimental results show a significant reduction of effective crosstalk compared to that of the conventional clock tree synthesis wherein crosstalk effect is not taken into account.

MPM1L-214 -- SPPV: A New Formal Verification Environment

Lubomir Ivanov and Michael Shute, *Iona College*

Formal Verification has become an integral part of the product development cycle leading to a demand for powerful, yet easy to use tools, which conceal the complexity of the underlying mathematical arguments through the use of convenient interfaces and automatic verification. In this paper we present a new formal verification environment ? SPPV ? based on series-parallel poset verification. SPPV allows fast, automated verification of event sequencing in complex systems. The system model and properties can be expressed as series-parallel poset expressions or in Verilog hardware description language.

MPM1L-216 -- VLSI Testing I
Monday: 2:00 pm – 3:20 pm
Chair: Mona Zaghloul
George Washington University

MPM1L-216 -- Substrate Coupling Fault Testing in System-on-a-Chip Digital Circuits

Henry H. Y. Chan and Zeljko Zilic, *McGill University*

Modern System-on-a-Chip (SoC) systems are implemented using deep submicron technologies and operate at the GHz range. Logic faults due to substrate coupling becomes a significant concern. Robust SoC designs must be able to predict and test substrate coupling hazards in the fabricated circuits. In this paper, we devise an efficient test pattern generation algorithm that identifies combinational logic faults due to substrate coupling. Faults are located based on cost functions applied to substrate parasitic models, which are generated by our substrate extraction tool. Fault coverage of the algorithm is verified with SPICE simulations.

MPM1L-216 -- A Hierarchical Test Access Mechanism for SoC and the Automatic Test Development Flow

Chao-Wen Chou, Jing-Reng Huang and Tsin-Yuan Chang, *National Tsing-Hua University*

Testing of the SoC takes a noticeable percentage of the overall cost, while accessing to the embedded cores is one of the key points in testing. In this paper, a hierarchical test access architecture that can interact with P1500 and TAP is proposed, and an computer-aided automatic test integration flow is built. Based on the minimum five I/O pins, the core under test is linked by semi-direct path with the external ATE during testing. For the core integrator, test patterns from the core provider can be transferred into the embedded core. Thus, it dramatically reduces the test integration effort and shortens the testing development time. The experiment results show that the effective test time overhead is about 1%.

MPM1L-216 -- Test Optimization of Bus-structured SoCs Using Embedded Microprocessor

Mohammad Tehranipour and Mehrdad Nourani, *University of Texas at Dallas,* and Mehdi Fakhraie, *University of Tehran*

Embedded processors are now widely used in system-on-chips. This paper presents an optimization technique for testing a bus-structured system using an embedded processor. We present a systematic approach for test access mechanism that allows processor to access all cores with minimum overhead. We show an ILP formulation to minimize the test schedule. The method requires negligible overhead but provides great flexibility in terms of access mechanism and future reuse.

MPM1L-216 -- A Petri-Net Approach to the Modeling and Analysis of Circuits and Systems with Applications to Test Generation for Digital VLSI

H. Kadim, *Liverpool JM University*

Technology today poses a great number of problems that require the construction of complex systems through specific arrangements of their components. This manifests itself in the complexity of testing, analysing and verifying VLSI systems. As a consequence of the development of highly complex systems, it is widely accepted that the lowest level approach is no longer feasible for VLSI. Hierarchy is a suitable structure for solving complex problems. In this work, Petri nets (PNS) are adopted as a modeling tool. They provide simple, accessible and powerful tools, which possess a wide variety of applications, for constructing models and solving problems. Based on the simple idea of transitions and places interconnected by arcs, PNS combine these basic elements into a rich assortment of forms and endow these forms with flexible properties, thus making the subject a useful tool for studying many kinds of systems

MPM1L-218 -- Wireless Networks I
Monday: 2:00 pm – 3:20 pm
Chair: John Metzner
Pennsylvania State University

MPM1L-218 -- Pulse Time Hopping for Multiaccess Communications with a Concatenated Code

John Metzner and Usana Tuntoolavest, *Pennsylvania State University*

An outer code decoding technique called vector symbol decoding has been shown to readily recognize correct symbol value choices on lists supplied by an inner code decoder. Pulse-time hopping multiaccess communication (and related fast frequency hopping) has a feature that there is a high likelihood the correct value appears on a short list. Under slow fading conditions, time-hopped pulses belonging to a particular sender are highly correlated as to shape and amplitude relative to interferers. An analysis shows that the combination of list decoding of pulse-time-hopped inner symbols with vector symbol decoding is highly effective.

MPM1L-218 -- Bluetooth and Wi-Fi: Enabling Coexistence

Jim Lansford and Rob Roy, *Mobilian Corporation*

This paper provides an introduction to issues of coexistence between Bluetooth and Wi-Fi (IEEE 802.11b), with particular attention to scenarios requiring simultaneous operation, or "Sim-OP," of both systems in very close proximity. The paper explains basic interference mechanisms and quantifies their impact through both actual measurements and simulation. The paper concludes with a discussion of techniques with the potential to greatly improve the performance of collocated Bluetooth and Wi-Fi systems.

MPM1L-218 -- Enhanced OFDM Time and Frequency Synchronization Through Optimal Code Correlation

Dongfang Liu and Jong-Moon Chung, *Oklahoma State University*

A pseudo-random noise (PN)-sequence synchronization method is proposed for orthogonal frequency division multiplexing (OFDM) time and frequency synchronization. By using a single PN-sequence as the first OFDM symbol, all synchronization can be accurately achieved. The peak correlation property of the PN-sequence makes time synchronization much more robust and accurate. Frequency synchronization precision is improved by averaging over the whole PN-sequence. At the same time, this method has a large frequency synchronization range. Finally, the residue time offset is estimated into the channel response.

MPM1L-219 -- Neural Networks with Non-linear Dynamics I
Monday: 2:00 pm – 3:20 pm
Chair: Damon Miller
Western Michigan University

MPM1L-219 -- Processing Temporal Sequences
Andrzej Lozowski and Bradley Noble *Southern Illinois University at Edwardsville*

We introduce a temporal sequence to be a signal composed of Dirac deltas separated by a sequence of time intervals. The choice of the Dirac delta representation has no meaning other than marking certain instances in time. More formally speaking, a temporal sequence x is a mapping Z -> R (integer-to-real), which resembles the set-theoretical definition of a sequence. Temporal sequences form a metric space. This allows for testing how close two temporal sequences are to each other. By defining a suitable metric, convergence of a dynamical system Z -> (Z -> R) can be tested. The meaning of the introduced dynamical system description is a temporal sequence undergoing iterations. This formalism is sufficient to investigate Cauchy convergence as well as synchronization of two temporal sequences. Completeness of the space or the existence of norm are not necessary properties at this point. Infinite countability of temporal sequences naturally arises from their definition. It is desirable from the point of view of engineering and signal processing. The existence of a countable basis set in the space is necessary for it to be Hausdorff, which has implications in terms of information storage capabilities. A temporal sequence memory will be investigated in the proposed paper from the perspective of engineering and implementation.

MPM1L-219 -- Indexed Families of Functionals, and Gaussian Radial Basis Functions
Irwin Sandberg, *University of Texas at Austin*

In this paper we report on results concerning the capabilities of gaussian radial basis function networks in the setting of inner product spaces that need not be finite dimensional. Specifically, we show that important indexed families of functionals can be uniformly approximated, with the approximation uniform also with respect to the index. Applications are described concerning the classification of signals, and the synthesis of reconfigurable classifiers.

MPM1L-219 -- A Hybrid Analog/Digital Circuit for Experiments in Controlling Chaos
Damon Miller, Michael Dozeman, Grant Westphal, and Ikhlas Abdel-Qader, *Western Michigan University*

This paper describes a circuit consisting of a chaotic oscillator, an analog-to-digital (A/D) converter, and a digital-to-analog (D/A) converter. The A/D converter is used to sample the oscillator output while the D/A converter generates a control voltage. Both the A/D and D/A converters are accessible to an external processor via a parallel port interface. The external processor is used to implement control strategies. As an example application this circuit is used to realize a chaotic associative memory as proposed in Jankowski et al. [1995].

MPM1L-219 -- Synchronization in a Pulse-coupled Network of Chaotic Spiking Oscillators
Hidehiro Nakano and Toshimichi Saito, *Hosei University*

In this paper, we present a pulse-coupled network of chaotic spiking oscillators. The system can exhibit various synchronous phenomena and asynchronous phenomena. Since the system is piecewise linear, the dynamics is analyzed by exact piecewise solutions. We give a basic classification of the synchronous phenomena and their breakdown patterns. Constructing a simple test circuit, typical phenomena can be verified in the laboratory. Finally, we discuss some application examples of our system.

MPM1L-221 -- Analog Signal Processing
Monday: 2:00 pm – 3:20 pm
Chair: Paul Hasler
Georgia Tech University

MPM1L-221 -- A Floating-Gate Vector-Quantization Circuit

Paul Hasler, Paul Smith, Chris Duffy, Christal Gordon, Jeff Dugger, and David Anderson, *Georgia Institute of Technology*

We present a floating-gate based circuit / system for computing vector quantization (VQ). VQ is typically used in data compression; for example in speech processing, VQ is used to reduce the set of detectable spectrum vectors to a manageable set for later classification. We present an architecture and resulting circuits which will enable direct programming / storage of weight vectors, as well as various methods for VQ weight adaptation. The circuit performing a continuous distance computation along a particular input coordinate is a variation on the analog bump circuit. Unlike a traditional bump circuit, we use differential floating-gate inputs to provide the ability to store the learned value. A cell outputs a maximum current if the two input values are nearly identical. These current outputs are summed along a single wire, where the largest result(s) are selected using a winner-take-all circuit. We present experimental results measured from ICs fabricated on a 0.5um CMOS process available through MOSIS. Our approach benefits from previous non-floating-gate VQ algorithms.

MPM1L-221 -- Development of a Post-Detection Equalization Technique for Multicarrier Modulation/Demodulation Systems

Luqing Wang, *University of Alberta,* and Behrouz Nowrouzian, *University of Alberta*

This paper is concerned with the development of a post-detection equalization technique for filterbank-based multicarrier modulation/demodulation systems. This technique is based on the equalization of the channel fractional delay in each subchannel in time synchronization with the constituent decimator at the receiver side. This time synchronization is achieved through the exploitation of a subset of the signal samples at the input of decimator (before downsampling). The resulting equalization gives rise to a high signal-to-noise ratio while requiring a small number of equalizer taps. Moreover, it permits a tradeoff between various equalization parameters, leading to high computational flexibility. The search for an optimal solution can be constrained to within the channel lower and upper group-delay bounds within each subchannel, resulting in a significant simplification in the equalizer training.

MPM1L-221 -- Synthesis of Translinear Analog Signal Processing Systems

Eric McDonald, *Cornell University,* and Bradley Minch, *Cornell University*

In this paper, we describe a structured methodology for synthesizing translinear analog signal-processing systems from high-level descriptions in the time domain. The circuits are implemented from elements called multiple-input translinear elements (Mites). We illustrate the synthesis methodology with a simple example.

MPM1L-221 -- Experimental Investigations of Floating-Gate Circuits in Sigma-Delta Modulators

Angelo Pereira, Philomena Brady, Abhishek Bandyopadhyay, and Paul Hasler, *Georgia Institute of Technology*

We present our initial experimental measurements using floating-gate structures in Sigma-Delta Analog-to-Digital Converters (ADC). We used floating-gate structures configured as e-pots as part of the modulator loop to provide convenient, and accurate programmable on-chip reference voltages. We use these e-pot outputs as tunable 1-bit DAC coefficients, which could be coupled with the ability to vary integrator gains. This approach is the first application of programmable floating-gate circuits towards Sigma-Delta converters. We see tunable coefficients allowing a designer to realize, within limits, a suitable noise shaping function, and achieve higher SNR. This approach results in a design of a sigma-delta ADC that is relatively tolerant to fabrication mismatches. As a result, this approach may improve loop stability and dynamics range of an ADC, particularly for higher-order modulators. Finally, using multiple programmable coefficients for several on-chip ADCs

results in immense benefits when building multi-channel, higher order modulators. We have fabricated a single loop, single bit, Sigma-Delta modulator, that is scalable to 8th order, to test these hypotheses. Experimental measurements were obtained from ICs fabricated in 0.5um process available through MOSIS. We use 16 e-pots in the ADC to implement the reference voltages for an 8th order modulator. The e-pots are implemented as a regular array structure discussed elsewhere. The chip operates from a single 5V supply.

MPM1L-223 -- Biomedical Signal and Image Processing I
Monday: 2:00 pm – 3:20 pm
Chair: Marios Pattichis
University of New Mexico

MPM1L-223 -- Conditional Anisotropic Diffusion For Leukocyte Identification
Dipti Mukherjee and Scott Acton, *University of Virginia*

Leukocyte identification is pursued in order to measure important parameters of inflammation including rolling leukocyte flux and rolling leukocyte volume fraction. The automated identification of leukocytes also serves as a precursor to leukocyte tracking. In this study, a conditional anisotropic diffusion model is used to enhance edges within video microscopy depicting rolling leukocytes within small venules. The detected edge chains are pruned according to the geometric information given in the leukocyte models, and candidate edge chains representing potential leukocytes are approximated by circular contours. The performance of the proposed approach is evaluated using images of TNF- treated venules within the mouse cremaster.

MPM1L-223 -- Real-time AM-FM Analysis of Ultrasound Video
Paul Rodriguez and Marios Pattichis, *The University of New Mexico*

An AM-FM video image representation is developed and applied to M-mode ultrasound. The fundamental AM-FM harmonic is estimated using a collection of bandpass filters. For each bandpass filter, the output image is downsampled depending on the spectral support of the filter. A fast separable implementation is implemented using only two separable, bandpass filters using the recently developed Single Instruction Multiple Data (SIMD) AM-FM video processing system. The fundamental AM-FM harmonic is seen to capture the essential structure of the image and simple thresholding of the amplitude estimate yields very good segmentation results.

MPM1L-223 -- Evaluation of Intravital Tracking Algorithms
Jinshan Tang and Scott Acton, *University of Virginia*

Tracking the motion of individual leukocytes (white blood cells) has been possible only in external flow chambers. We are attempting to investigate the feasibility of tracking leukocytes in vivo. Three tracking algorithms have been developed for tracking leukocytes: normalized cross-correlation tracking, centroid tracking and active contour (snake) based tracking. This paper focuses on the analysis, the evaluation and the comparison of the above three tracking algorithms using some performance measures. These performance measures include: (1) the average number of consecutive frames racked, (2) the localization error, (3) a novel signal-to-clutter ratio (SCR), and (4) registration error per sequence. One hundred in vivo videos were used in our experiments for analysis, evaluation and comparison. The results lead to three key findings: the in vivo tracking problem is significantly more difficult than the in vitro tracking problem; the snake based tracking provides the most robust solution of the three algorithms tested, and the automated tracking system can replace the manual tracking of leukocytes.

MPM1L-223 -- Spatial Image Variability Analysis

Marios Pattichis, *The University of New Mexico*, Theophilos Cacoullos, *The University of Athens and The University of New Mexico*, and Pete Soliz, *Kestrel Corporation*

In our analysis, each image is partitioned into a number of non-overlapping, spatial regions, and a grade (0/1) is assigned to each region, by two independent graders. Here, 1 represents success, while 0 represents failure to detect a hypothesized pattern in the region. For each rater, we compute the likelihood of each spatial distribution of grades, and we rank the spatial distributions from the most likely to the least likely. We also compute the spatial regions, with associated estimated probabilities, where hypothesized patterns are present. This analysis is applied to Computer Assisted Diagnosis.

MPM1L-225 -- Coding for Comunications
Monday: 2:00 pm – 3:20 pm
Chair: Monique Fargues
Naval Postgraduate School

MPM1L-225 -- Condensed Huffman Coding, A New Efficient Decoding Technique

Reza Hashemian, *Northern Illinois University*

A new technique is proposed for decoding Huffman codes. In this technique a Condensed Huffman Table (CHT) for decoding purposes replaces a typical Huffman table. It is shown that a CHT is much smaller in size and the decoding becomes significantly faster. In an example with a typical Huffman table containing 108 codewords, it is shown that a CHT with only 14 codewords is sufficient to perform the decoding.

MPM1L-225 -- An Efficient Macroblock-Sync Decoding Architecture for MPEG-4 FGS Video

Hsi-Kang Tsao, *National Taiwan University*, Yi-Shin Tung and Ja-Ling Wu, *NTU CSIE*

MPEG-4 amendment 2 provides a new coding technique, Fine Granularity Scalability (FGS), which provides the fine-granular rate adjustment capability. This property meets the growing need of streaming video over bandwidth-varying environment. By coding bitplanes of DCT residues from the most significant bit (MSB) to the least significant bit (LSB), FGS makes the compressed bitstream able to be truncated at any location. The resultant video quality would gradually be refined with the increase of the received bitstream. However, an extra frame buffer for storing bit-values of decoded DCT residues and several times of buffer scanning/accessing for accumulating these residues make FGS difficult to be implemented efficiently, especially in memory-constraint system (for example, PDA, smart phone and TablePC). In this paper, we present a Macroblock-Sync decoding process for FGS decoding, which reduces the extra buffer requirement and decreasing the memory-access frequency at the same time. In our design, all processes of the same macroblock (originally done in the base and enhancement decoders respectively) are operated simultaneously. The proposed decoding architecture provides a distinct data-access order and results in a better cache utilization, which overcomes the two-abovementioned problems when realizing the FGS decoder. In our experiments, up to 80% speed-up can be achieved.

MPM1L-225 -- Communication Security Using Chaotic Generator

Abdelatif Elkouny and Mohamed Sobhy, *Kent University*

This paper presents an encryption algorithm that can be used for text messages, images and recorded voice with high security. The proposed algorithm is then applied for secure communication using a new approach for constructing two chaotically synchronized systems in the presence of a channel delay. The simulation results reveal that synchronization and a signal to chaos ratio of -252dB have been achieved.

MPM1L-225 -- SPIHT Implemented in a XC4000 Device

Jörg Ritter, Görschwin Fey, and Paul Molitor, *Martin-Luther-University Halle-Witttenberg, Germany*

In this paper we present an efficient FPGA implementation of the 'Set Partitioning in Hierarchical Trees' (SPIHT) algorithm of Said and Pearlman in combination with an arithmetic coder. The FPGA implementation is applied within a partitioned approach for wavelet-based lossy image compression. The basic SPIHT algorithm uses dynamic data structures that make a hardware realization difficult. We illustrate in detail how these dynamic data structures can be implemented in the FPGA without the use of external memory. We present a hardware realization which can be run with a frequency of 40~MHz in a Xilinx XC4000 device. The design requires 23% less internal memory as the recently published algorithm 'SPIHT Image Compression without Lists' of Wheeler and Pearlman.

MPM1P-140 -- Sensors, Analog Filters, and Data Conversion
Monday: 2:00 pm – 3:20 pm

Chair: Sherif Michael

Naval Postgraduate School

MPM1P-140 -- Comparison of Analytical and Numerical Models with a Novel Computer-based Model, for the Prediction of Semiconductor Freeze-out and Exhaustion Regimes

Ron Pieper, Sherif Michael, and Derek Reeves, *Naval Postgraduate School*

Silvaco International software is well designed to solve the electron/hole transport problem, which can typically lead to the device IV characteristic. On the other hand, to obtain a temperature dependent plot for majority carrier concentration for a uniform semiconductor can, surprisingly, be somewhat complicated from a procedure viewpoint. Our paper will present an efficient novel way of obtaining this curve from the Silvaco software and compare the results with a proposed one dimensional single-equation analytic model and a numerical model that predict the temperature dependence for majority concentration in all regimes numerical model.

MPM1P-140 -- A Monolithic Time of Arrival Detector for Acoustic Signals

Michael Obara, Godi Fischer, and Sangmok Lee, *University of Rhode Island*

This paper describes the design and implementation of a time of arrival detector for long-range underwater acoustic signals. The intended application of this device is a tag for acoustically tracking aquatic animals, but it is suited for computing general low-frequency signal arrival times in an underwater environment. This device is optimized for low SNR as well as Doppler insensitivity. The two main components of the detector are an analog multi-rate filter, and a digital correlator. The analog filtering is realized by three second order switched-capacitor filter stages. The digital correlation consists of 2048 bits of static RAM (SRAM): 1024 bits to store the expected pattern and 1024 as a virtual shift register. Due to the nature of the intended application, power consumption must be kept to a minimum. Two prototype dies have been fabricated by a 0.5um double-poly CMOS process. The filters were shown to operate at under 1.5uA per stage and the SRAM to operate correctly.

MPM1P-140 -- Design of KHN Biquad using Operational Transconductance Amplifiers

Sameena Shah, and Data Ram Bhaskar, *Jamia Millia Islamia*

The proposed circuit improves the frequency response, power dissipation and supply range of the KHN biquadratic circuit. It uses a minimum number of Operational Transconductance Amplifiers (OTAs) to achieve the same. The various parameters namely center frequency, dc gain, Bandwidth, Power Dissipation and Quality factor are all electronically tunable. Simulations are included to verify the analysis.

MPM1P-140 -- New Genetic Algorithm Approach For Dynamic Biochemical Sensors-Measurement Characterization

Deepak Gantla, *MSDL/Oakland University,* and Hoda Abdel-Aty-Zohdy, *Oakland University*

In this paper we present a Genetic Algorithm for measurement characterization with dynamic inputs. Dynamic inputs represent real life sensor measurements (readings from biochemical sensor arrays.) Input signals (measurements) are assumed in parallel from biochemical sensor arrays. An input multiplexer/controller/Analog-Digital converter preprocessing stage is used to control the flow of input measurements. The new GA approach considers input signals as 128 controlled parallel measurements. The new dynamical approach presents measurement characterization and also optimum fused measurements without sacrificing the integrity of incoming signals. This is achieved by assigning initial random weight to each feature of each incoming sensor measurement. Vectors of these weights are considered the chromosomes in our evolutionary approach. Through a novel mutation and crossover approach (Half Sibling and A Clone) optimum characteristic weight chromosomes are achieved. In olfaction system (E-Nose) hardware implementation, outputs from the GA approach are used as inputs to an Intelligent Neural Network System for biochemical detection and decision-making. An effective mutation and crossover scheme Half Sibling and A Clone (HSAC) has been developed, simulated, and implemented. The HSAC approach is applied at various iteration levels and kept a dynamic error to a minimum. By this scheme, a single converging chromosome value is achieved within less than 10 iterations. Hardware implementation and minimization has also been considered while developing the new GA approach. Simulation results of the new GA with dynamic measurements are satisfactory and will be presented. An added key feature of the approach is that no pre-assigned minimum error is required, rather, error is dynamically evaluated based on measurements. MATLAB has been used as the simulation tool. Hardware implementation in a digital FPGA system, and performance evaluation will also be presented.

MPM1P-140 -- Feedforward Current-mode Allpass Circuits

Peter Aronhime and Tongfeng Qian, *University of Louisville,* and Brent Maundy, *University of Calgary*

A feedforward configuration for realizing second-order voltage-mode allpass transfer functions with complex poles using voltage-mode op-amps is converted to a feedforward current-mode scheme for the realization of second-order current-mode allpass transfer functions with complex poles using current conveyors. The scheme is capable of generating many different realizations for allpass transfer functions. Several new realizations are presented, and the effects of parasitic elements associated with the current conveyors in one realization are analyzed in detail. Simulations and laboratory measurements are provided.

MPM1P-140 -- Analog Multiplexing in Time Domain for Biochemical Measurement Processing

Apurva Patel and Tara Terry, *MSDL/Oakland University,* and Hoda Abdel-Aty-Zohdy, *Oakland University*

Digital multiplexers have seen significant amount of research and widespread applications. Analog multiplexers, through the use of filters, has also seen substantial, but less than digital, amounts of research and applications and although there are applications that have implemented analog multiplexers, they have been implemented in the frequency domain, which requires extensive hardware and is costly, whereas an analog multiplexer in time domain is considered in this paper. This paper presents Design, Simulation, Implementation and evaluation of a 4:1 analog multiplexer. The analog multiplexer is implemented with the help of four buffers and four transmission gates. The implemented buffers uses NMOS saturated load transistor implemented in 0.35mm CMOS technology, with optimum linear ranges for the analog input and output signals. Designed multiplexer has up to 66% linear range of the supply voltage. The analog multiplexer is developed for a biochemical preprocessing unit to multiplex time-varying analog input signals coming from real-time sensor arrays and to connect the selected input to one A/D converter for digital implementation of a bio-inspired intelligent signal detection and processing system, or for an analog implemented biochemical detection system. Using an analog multiplexer will decrease the number of A/D converters required for a large number of analog inputs, efficiently reducing the effective cost of facilitation for real-time on-the-spot hazardous/toxic detection and decision making.

MPM1P-140 -- Class AB VHF CMOS Active Inductor

Apinunt Thanachayanont, *King Mongkut's Institute of Technology, Ladkrabang*

A class AB VHF CMOS active inductor with increased signal handling capability is described. Comparing to a class A circuit with the same inductance value, Q factor, and power dissipation, the proposed circuit achieves about 12-dB improvement in dynamic range while maintaining high-frequency operation. Further enhancement is also obtained by using a fully differential floating inductor. HSPICE simulation using BSIM3V3 model with 0.35-mm process parameters shows that the fully differential floating active inductor achieves a 51.8-dB dynamic range while dissipating 2.7 mW from a +/-1.5 V supply voltage.

MPM1P-140 -- Offset Cancellation and 1/f Noise Suppression for Chopper Amplifiers

Rajan Walia, Yu Fei Pan and Boon Seah Quek, *Institute of Microelectronics*

This paper describes a scheme to suppress modulated offset of chopper amplifier by using synchronous demodulation and subtraction. The operation is based on continuous time extraction of offset information from chopper output and generation of correction signal to be fed back to the auxiliary input of chopper amp. Analytical and simulation results show that not only input referred offset is reduced buts also 1/f noise is suppressed.

MPM1P-140 -- Modified Elliptic Filters with Improved Delay Response and Sensitivities and Pole Qs

David Báez-López, *Universidad de las Américas-Puebla*

We present a design technique for transformed lowpass elliptic filters. For this purpose we use a transformation to reduce the number of maxima in the passband frequency response. The transformed elliptic filter has an improved group delay response and it also has improved sensitivities.

MPM1P-140 -- Investigating Programmable Floating-Gate Digital-to-Analog Converter as Single Element or Element Arrays

Guillermo Serrano, Matt Kucic, and Paul Hasler, *Georgia Institute of Technology*

This approach takes the classical scaled transistor DAC techniques, where we scale our transistors by programming each transistor's floating-gate charge instead of W/L ratios. The programming eliminates device mismatch issues on DAC performance. We investigate the feasibility of this approach by making experimental measurements from fabricated floating-gate DAC circuits. The resulting structure requires minimal IC area, since it only uses a minimum or nearly minimum size transistor and a capacitor per bit of resolution.

MPM1P-140 -- Design of Oversampling Sigma-Delta DAC for ADSL Applications

Sun-Hong Kim and Seok-Woo Choi, *Chonbuk University*, Chang-Hun Yun, *Woosuk University*, Byoung-Wook Kim, and Dong-Yong Kim, *Chonbuk University*

A transceiver for ADSL systems contains an interpolated combfilter, halfband filters, oversampling sigma delta modulator, a current steering DAC and an analog filter. The circuit complexity of the architecture makes it necessary to use behavioral models to determine the system features. For this reason, we need a specific behavioral simulation environment using the MATLAB program. The MATLAB is crucial for these circuits to be rapidly incorporated in larger systems, in particular in the context of mixed-signal-test schemes. Design trade-off among the blocks has also been discussed. The design methodology is based on behavioral design and CMOS process.

MPM1P-140 -- Efficient Use of Two-Path Filter in The Low Power Decimation Filter Design

Xunyu Zhu, Chris Hutchens, and Chia-Ming Liu, *Oklahoma State University*

This paper compares three design methods for decimation filters that are used with delta-sigma modulators. Comparison is from power dissipation, layout area, and design time. Both simulation results and field measurement shows that Type 3 filter is the most efficient way for low-power decimation filter design.

MPM1P-140 -- CMOS Design and Implementation of Sigma-Delta Analog-to-Digital Data Converter suitable for MEMS Devices

Mona Zaghloul and Anis Nordin, *The George Washington University*

MicroElectroMechanical systems (MEMS) are rapidly gaining popularity over a wide range of applications today [6]. An example of full integration in MEMS is the smart sensor where both the sensors and the electrical signal -processing circuitry are placed on the same chip. The idea is to place the sensor as close as possible to the signal-processing interface to avoid signal degradation. In this paper we present the design and implementation of an interface circuit for CMOS sensor systems. A first-order sigma-delta analog-to-digital converter was designed and simulated using Cadence and SpectreS. An experimental prototype of the 10-bit sigma-delta modulator was then fabricated using 1.6um CMOS technology through MOSIS.

MPM1P-140 -- An Algorithm for Dividing Ambiguity Sets for Analog Fault Dictionary

Jinyan Cai and Mohammad Alam, *University of South Alabama*

A new algorithm for dividing ambiguity sets based on the lowest error probability for analog fault dictionary is proposed. The problem of tolerance affecting diagnostic accuracy in analog circuits is discussed. A statistical approach is used to derive the probability distribution of the tolerances of the output signal characteristics both in the absence and in the presence of faults in the circuit. For example, in this paper, Monte Carlo technique has been applied for the analysis of tolerance. The lowest error probabilities are computed according to Bayesian strategy. Using the PSpice software package, a detailed simulation program was developed to implement the proposed technique. The simulation software was packaged and then integrated with a symbolic analysis program that divides the ambiguity sets and structure the software package for the analysis before testing in the fault dictionary. Furthermore, the proposed approach can be easily extended to select the testing nodes leading to the selection of optimized nodes for the analog fault diagnosis.

MPM2L-209 -- Amplifiers II
Monday: 3:40 pm – 5:00 pm
Chair: Mark Schlarmann
Iowa State University

MPM2L-209 -- New Architectures of Class AB CMOS and BiCMOS Op-Amps with Local Common Mode Feedback

Michael Holmes and Jaimie Ramirez, *New Mexico State University*

It is shown that utilization of local common mode feedback in one stage op-amps can provide significant improvement in the slew rate and gain bandwidth with the same silicon area and static power dissipation. A comparison of one stage CMOS and BiCMOS single ended and fully differential architectures with and without local common mode feedback is presented. Experimental and simulation results are shown that verify the expected performance improvements.

MPM2L-209 -- Low Voltage Fully Differential Opamp with High Gain Wide Bandwidth suitable for Switched Capacitor Applications

Sherif Hammouda and Mohamed Tawfik, *Mentor Graphics,* and Hani Ragaie, *Ain Shams University*

In this paper the design of a low voltage fully differential amplifier operating from 0 to 1.5 V single supply is presented. The amplifier has the advantages of having very high gain, wide bandwidth, a fast settling time and a high output swing. The amplifier presented was designed in a 0.35um CMOS technology. The complete design of a switched capacitor lossy integrator based on the proposed amplifier is presented. The proposed switched capacitor integrator can function in very low voltage without using voltage boosting or switched-opamp techniques.

MPM2L-209 -- A Low-Voltage Body-Driven CMOS Transconductor

Xuguang Zhang and Ezz El-Masry, *Dalhousie University*

A novel low-voltage triode-mode CMOS transconductor is presented. Enhanced linearity and tuning range are achieved by implementing body-driven technique and gain-enhancement scheme. Simulation results using 0.18um N-well CMOS technology confirm the superior performance of this transconductor. With 1.5 V single power supply, the transconductor is linearly tunable over one decade. For differential input signal with peak amplitude up to 0.4 V, the THD is less than -50 dB for the entire transconductance tuning range. The proposed highly linear transconductor is suitable for realizing continuous-time filters with reduced power supply.

MPM2L-209 -- Yield Enhanced Layout Strategies for Ratio Critical Analog Circuits

Yu Lin, Saqib Malik, and Randall Geiger, *Iowa State University*

A yield enhanced layout method for maximizing yield of integrated resistor networks with a fixed total area is discussed. This approach incorporates both random variations in the sheet resistance and random variations in the contact resistances. The concept of contact/sheet resistance crossover which gives the crossover between contact-resistance dominance and sheet resistance dominance is developed.

MPM2L-211 -- RF and Microwave Oscillators II
Monday: 3:40 pm – 5:00 pm
Chair: Yumin Zhang
Oklahoma State University

MPM2L-211 -- A Comparative Study of CMOS-based Quadrature Integrated LC VCO Topologies

Khalid Sharaf and Hani Ragai, *Ain-Shams University*, and Hazem Hegazy, *Mentor Graphics*

Topologies comparison of a 1GHz quadrature voltage controlled oscillator, VCO, based on simulation results is presented. VCO circuits are simulated using 0.25micron CMOS process from 2.5V supply. The comparison is introduced from two different perspectives: constant VCO DC power and constant output swing. The main differences between different topologies seeking same targeted VCO specifications are shown.

MPM2L-211 -- A Non-Feedback Multiphase Clock Generator Using Direct Interpolation

Lixin Yang, Yijun Zhou, and Jiren Yuan, *Lund University*

This paper presents a new multiphase clock generator using direct interpolators. No feedback loop is required. A single-stage direct interpolation architecture is proposed. A 1/4 frequency divider and a short-circuit current suppression interpolator are developed to achieve the precise interpolation. The circuit was fabricated in a standard 0.35mm, 3.3V CMOS process. The multiphase clock generator can operate in a wide range of input clock frequencies from 500 MHz to 1 GHz.

MPM2L-211 -- Optimal Loop Parameter Design of Charge Pump PLLs For Jitter Transfer Characteristic Optimization

Hanjun Jiang, Chengming He, Degang Chen, and Randall Geiger, *Iowa State University*

An optimal loop parameter design method of charge pump PLLs for jitter transfer characteristic optimization is proposed. Based on the linear model of charge pump PLLs, the relationship between PLLs/loop parameters and jitter transfer characteristic is illustrated. Using the proposed optimal design method, a design example is done and the expected simulation result is obtained.

MPM2L-211 -- Analysis of DLL Jitter Due to Substrate Noise

Payam Heydari, *University of California*

Substrate noise is the major source of performance limitation in mixed-signal integrated circuits. This paper studies substrate noise effects on the performance of delay-locked loops (DLLs). Due to their robust noise performance, the delay-locked-loops are widely used as clock generators of microprocessors. Although exploiting advanced circuit techniques reduces the timing jitter induced by the substrate noise to a large extent, the hostile noisy digital section in a mixed-signal VLSI circuit can still cause a large substrate noise and hence a non-negligible timing jitter in DLL clock generators. In this paper a new stochastic model for the substrate noise is proposed. This model is then utilized to derive the phase noise of the voltage-controlled delay line (VCDL) inside the loop. The DLL timing jitter is predicted in response to the VCDL phase noise. A comparison between the results obtained by our mathematical model and those obtained using HSPICE verifies our proposed model.

MPM2L-213 -- Oversampled Data Conversion II
Monday: 3:40 pm – 5:00 pm
Chair: Kwong Chao
Texas Tech University

MPM2L-213 -- A Parallel Digital Architecture for Delta-Sigma Modulation
Dan Scholnik, *Naval Research Laboratory*

A major drawback of delta-sigma modulation is the high oversampling ratios required, especially for single-bit quantization. Accordingly, much of the research in the area has focused on lowering the sampling rate through various parallelization approaches. However, this research has been overwhelmingly concentrated on continuous and discrete-time analog modulator implementations for A/D converters, and not on reducing the critical path in a digital implementation for D/A conversion. In this paper the popular time-interleaved modulator is paired with a vector quantizer implementation of a finite-length modulator to form a parallel implementation of a delta-sigma modulator with a reduced critical path.

MPM2L-213 -- Delta-Sigma Modulator Topologies for High-Speed High-Resolution A/D Converters
Anas Hamoui and Ken Martin, *University of Toronto*

By fully exploiting the enhanced stability characteristics of multibit quantization, stable higher-order delta-sigma (DS) modulators with finite-impulse-response (FIR) noise-transfer-functions (NTF) can be designed to achieve high signal-to-quantization-noise ratios at low oversampling ratios (OSR). This paper proposes a multibit DS modulator topology to realize FIR NTFs of arbitrary orders. Its key features include: reduced sensitivity to integrator nonlinearities, improved robustness to DS modulator coefficient variations, and decreased circuit complexity. Its performance is validated through simulations and compared to traditional DS modulator structures. This paper further discusses how the design of the signal transfer function (the signal path within the DS modulator) can significantly reduce the harmonic distortion due to opamp nonidealities in the modulator's loop filter and can help reduce the power dissipation, especially for high-speed high-resolution analog-to-digital converters (ADC) designed in low-voltage fine-line technologies.

MPM2L-213 -- Mismatch-insensitive N-path Multirate Sigma-delta Modulator for High-frequency Applications
Fan Lou, Seng-Pan U, and Rui Paulo Martins, *University of Macau*

An N-path multirate Sigma-Delta Modulator (SDM) was recently proposed where the first integrator was implemented using an N-path architecture and a comb filter. The replacement of the first integrator in the N-path structure and the comb filter can relax the speed requirements of the opamps in the first stage and alleviate various mismatch effects. An improved structure for the comb filter is proposed here which eliminates thoroughly the mismatch effects between paths. Analysis and simulations also show that the proposed structure makes the N-path multirate SDM more stable and mismatch insensitive.

MPM2L-213 -- MSE Law of nth Order Sigma-Delta Modulators
Nguyen T. Thao, *City College*

The mean squared error (MSE) of an nth order Sigma-Delta modulator is classically understood to decay with the oversampling ratio M at the rate alpha/M^(2n+1). In this paper, we show that the accurate general MSE law is in fact in beta/M^(2n)+gamma/M^(2n+1) instead. The coefficient beta is in general not zero, except when the input is rigorously constant, or when using the ideal standard nonoverloaded n-bit n-loop modulator. The term beta/M^(2n) is dominant starting from low values of M when using a one-bit quantizer.

MPM2L-214 -- VLSI: Power, Noise, and Simulation II
Monday: 3:40 pm – 5:00 pm
Chair: Peter-Michael Seidel
Southern Methodist University

MPM2L-214 -- Analyzing the Simultaneous Switching Noise Due to Internal Gate Switching

Li Yang and JiannShun Yuan, *University of Central Florida*, and Michael Hagedorn, *Theseus Logic*

In this paper, the ground bounce noise due to internal gate switching is studied. It has been found that both power-rail and ground-rail pin impedances are important in evaluating internal ground bounces. Based on the lumped-model analysis taking into account the parasitic effects of MOS transistors, a novel analytical model is developed which accurately accounts for both power rail and ground rail pin models. The proposed model is compared with the previous work and validated by SPICE simulation results.

MPM2L-214 -- Analysis and Algorithms for Scheduling with Minimal Switching Activity

Edwin Sha, *University of Texas at Dallas*

Switching activity is one of the important factors in power minimization. This paper studies the scheduling problem which minimizes the switching activity. We show that to find the schedule which minimizes switching activity only or minimizes latency and switching activity with or without resource constraints is NP-complete. Two heuristic scheduling algorithms to minimize the switching activity are presented. The algorithms use the weighted bipartite matching to find a good schedule. The experimental results show that our algorithms can produce the near-optimal schedule which uses averagely the switching activity 35% less compared to the traditional list scheduling.

MPM2L-214 -- A Wire Load Model For More Accurate Power Estimation

Armin Windschiegl, Paul Zuber and Walter Stechele, *Technische Universität München*

The wire load of the interconnections of standard cells is an important variable for use in power and timing analysis and, in the last years, especially for concurrent synthesis and placement optimization tools. On the one hand wire load models are characterized by pre-layout wirelength estimations and capacitance per unit length is modeled as "weighted average over all metal layers". On the other hand pre-layout wirelength estimations are very inaccurate and the layer-specific capacitances are very different. As a consequence significant errors are caused when using wire load models for power estimations. In order to improve the accuracy of power estimation on gate level, we present a methodology for the generation of wire load models for standard cell designs in modern deep-submicron technologies with six metal layers.

MPM2L-214 -- A Statistical Model of Input Glitch Propagation and Its Application in Power Macromodeling

Xun Liu and Marios Papaefthymiou, *University of Michigan*

Power macromodeling technique can result in huge underestimation without the consideration of input glitches. In this paper, we propose a statistical model for the propagation of input glitches and their effects on circuit power consumption. Based on this model, we develop an analytical power macromodeling approach incorporating input glitches. Specifically, we divide the macromodel parameter space into three regions and characterize each region separately. We have evaluated the proposed technique on ISCAS85 and LGSynth93 benchmark circuits. Compared with switch level simulation results, the average power estimation errors are 1.8% and 3.1% for combinational and sequential circuits, respectively. Our model also provides useful insight for glitchy circuit identification and input glitch power reduction.

MPM2L-216 -- VLSI Testing II
Monday: 3:40 pm – 5:00 pm
Chair: Mona Zaghloul
George Washington University

MPM2L-216 -- An Analog Mixed-Signal Test Controller

Mohammed AbdEl-Halim, *Mentor Graphics*

A Design For Test (DFT) technique for analog mixed-signal (AMS) system on a Chip (SoC) is presented; both methodology and implementation are introduced. Using the IEEE boundary scan standard 1149.4, small embedded analog test controller (ATC), and utilizes the embedded SoC memory. Using this structure almost any AMS-SoC can be tested for both manufacturing, off-line, and on-line tests. This technique relaxes the tester requirements and enables cost effective on-line testing.

MPM2L-216 -- State-Space based Transient Faults Analysis for VLSI Circuits and Systems

H. Kadim, *Liverpool JM University*

The dynamic behaviour of analogue circuits can be represented by a number of transient responses corresponding to poles in the complex plane. Abnormalities in circuit behaviour may not be detected at the functional level since transients may mask the effects of parametric faults. The method proposed in this paper considers the behavioural verification of analogue circuits in both the time domain and the frequency domain based on investigations into the characteristics of the decoupled poles.

MPM2L-216 -- A Test Method And DFT Structure For Analog Modules In Mixed-Signal Circuits

Mahmoud Al-Qutayri, *Etisalat College of Engineering*

This paper outlines the difficulties associated with testing analog circuits in general and those residing within mixed-signal circuits in particular. It proposes a system level oriented tested method based on the excitation of the circuit-under-test with a pseudo random binary sequence and the subsequent analysis of the captured response. The fault detection capabilities of the test and data analysis methods are demonstrated by simulation results. The effect of the test sequence length on fault detection is studied. It also discusses a design for testability structure that can be incorporated in a mixed-signal chip to enable the testing of the analog circuit blocks.

MPM2L-216 -- NCR: A Self-scaling, Self-calibrated Metric for IDDQ Outlier Identification

Sagar Sabade and Duncan Walker, *Texas A&M University*

IDDQ testing is an important component of a test suite. However, increasing leakage current values with each technology node render single pass/fail limit setting approach obsolete. This is further worsened due to increasing process variations. Discriminating faulty chips from fault-free chips is becoming increasingly difficult. In this paper we present a metric that uses wafer level spatial information to identify faulty dice on a wafer. The metric is evaluated using industrial test data.

MPM2L-218 -- Wireless Networks II
Monday: 3:40 pm – 5:00 pm
Chair: John Metzner
Pennsylvania State University

MPM2L-218 -- Reliable Satellite Multicast with Assistance of Terrestrial communications
Mei Li and John Metzner, *Pennsylvania State University*

Satellite networks can distribute data to a large number of receivers. Traditional automatic repeat request (ARQ) requires retransmission until all receivers obtain the correct packets. If packet error rate is high on the satellite links, retransmissions consume a lot of satellite bandwidth and delay is large. This paper proposes a method to correct the erroneous or lost packets by terrestrial communications. This reduces retransmission via satellite. Several topologies and methods are proposed to minimize the terrestrial communications. Analytical results demonstrate that a ring model has the best performance among the proposed topologies.

MPM2L-218 -- A Mobility Enhancement for Switched Wireless Ethernet with Soft Handoff
Raheem Beyah, *Georgia Institute of Technology,* Corey Turner, *Cisco,* Cherita Corbett and John Copeland, *Georgia Institute of Technology*

With the proliferation of mobile users, wireless LANs (WLANs) are quickly entering enterprise networks. These networks have traditionally been configured in a Shared Ethernet topology. Due to the tremendous performance increase over Shared Ethernet, most corporations' networks are slowly being migrated to a Switched Ethernet topology. Traditional Ethernet switches will not suffice to completely take advantage of this WLAN technology. When WLAN's use Ethernet switching as a backbone, service disruption may occur when attempting to migrate from one cell to another. This disruption does not occur on Shared Ethernet networks. The authors propose a soft handoff procedure to ensure optimal performance, minimal service disruption, as well as minimal broadcast frames.

MPM2L-218 -- Bluetooth Handover Control for Roaming System Applications
Moses Lynn George, Lijy Jose Kallidukil, Moon-Moon Chung, *Oklahoma State University*

Bluetooth has emerged to be a low cost technology that could be targeted at wireless applications with not so long range varying between 1 to 100 meters. To provide uninterrupted service while moving around continuously among different piconets, an efficient Handover technique has not been developed yet. The paper discusses three methodologies that could be used to provide soft handover of a BT device between different masters or Base Stations. The key principles of Handover in Bluetooth lies in finding the Bluetooth address of the device to connect to and synchronize fast enough to it, to reduce connection time.

MPM2L-219 -- Neural Networks with Non-linear Dynamics II
Monday: 3:40 pm – 5:00 pm
Chair: Damon Miller
Western Michigan University

MPM2L-219 -- A Biologically Motivated Paradigm for Scene Segmentation
Liang Zhao, *University of Sao Paulo,* and Elbert Macau, *Brazilian National Institute for Space Research (INPE)*

In this paper, we propose a new paradigm to solve the scene segmentation problem. This paradigm is neurophysiological based and exploit the physical properties of a network of dynamically coupled chaotic maps to accomplish scene segmentation. Thus, an object in a scene is associated to synchronized time evolutions of

chaotic maps, while different objects are discriminated by different sets of synchronized chaotic maps that are desynchronized with one another. In our paradigm, the coupling range of each active element increases dynamically according to predefined rules until a saturated state is achieved, i.e., locally coupled chaotic maps corresponding to an object in the initial state will be coupled globally in the final state. Computer simulations that support our paradigm are presented.

MPM2L-219 -- Determining the Network Parameters of the Amphibian Vision System

Elizabeth Brauer and Kiisa Nishikawa, *Northern Arizona University*

The objective of this research is to develop vision systems based on visual predators of the amphibian family (toads, frogs and salamanders). The initial phase of the project is modeling a retina (R2, R3, R4) and several neuron layers (T3, and TH-1), and their inhibitory and excitatory synapses using Genesis, a general purpose neural simulator. Since the network parameters are unknown, we are using genetic algorithms to search for a combination of parameters that produces the desired output of correctly identifying prey.

MPM2L-219 -- Unsupervised Classification Using Associative Memory

Mohammad Sayeh, *Southern Illinois University*

This paper reviews an associative memory based on ordinary differential equations. The unsupervised-classification application of this system is discussed. Some examples are given.

MPM2L-219 -- Design of a Pipelined Hardware Architecture for Real-Time Neural Network Computations

Jose Ayala, Antonio G. Lomeña, Marisa Lopez-Vallejo, and Angel Fernandez, *Universidad Politecnica de Madrid*

In this paper, we present a digital hardware implementation of a Neural Network server. The key characteristics of this solution are on-chip learning algorithm implementation, sophisticated activation function realization, high reconfiguration capability and operation under real time constraints. Experimental results have shown that our system exhibits better response in terms of recall speed, learning speed and reconfiguration capability than other implementations proposed in the literature. Additionally, an in depth analysis of data quantization effects on network convergence has been performed and a set of design rules has been extracted.

MPM2L-221 -- DSP in Communications
Monday: 3:40 pm – 5:00 pm
Chair: Paul Hasler
Georgia Tech University

MPM2L-221 -- An New Interpolation Equalization Scheme for Discrete Wavelet Multitone Modulation/Demodulation Systems

Luqing Wang and Behrouz Nowrouzian, *University of Alberta*

Discrete Wavelet Multitone (DWMT) Modulation provides an alternative to the conventional Discrete Multitone (DMT) Multicarrier Modulation in various Digital Subscriber Line (xDSL) applications. In this paper, by taking into account the dominant effects of the noninteger channel delay, the conventional pre- and post-detection equalization techniques are combined to obtain a novel interpolation equalization scheme. Simulation results show that the proposed technique results in a relative high Signal-to-Interference Ratio (SIR) and low computation complexity with one-tap interpolation equalization, permitting a high achievable SIR.

MPM2L-221 -- Clustering-based Blind Maximum Likelihood Sequence Detection for GSM and TDMA Systems

Deepak Boppana and Sathyanarayana S Rao, *Villanova University*

A novel blind maximum likelihood sequence detector (MLSD) for GSM and TDMA based systems is proposed. The baseband data at the receiver are partitioned into clusters that are identified using a new class of unsupervised clustering algorithms known as K-Harmonic Means (KHMp). The KHMp algorithms are insensitive to the initialization of the cluster centers owing to a built-in boosting function, and thus provide reliable estimates of the cluster centers. The identified cluster representatives are then mapped to the corresponding combinations of input symbols using a discrete hidden Markov model formulation of the channel states and the mapping is used to compute the branch metrics in a cluster-based MLSD to perform signal detection. The proposed detector avoids any explicit channel modeling and training overhead and its performance is evaluated for the GSM systems.

MPM2L-221 -- A Novel Approach to Fast DOA Estimation of Multiple Spatial Narrow-band Signals

Liang Tao, *Anhui University*, and H Kwan, *University of Windsor*

A novel approach, which is totally different from the traditional methods, for estimating directions-of-arrival (DOA) of multiple spatial narrow-band signals is presented in this paper. Based on fast Fourier transforms (FFT) of the sensor array output data, a relationship between the FFT spectrum and direction-of-arrival angles is established so that the angles can quickly be estimated through searching peaks in the FFT spectrum. In addition, the performance of the proposed approach with sensor gain and phase perturbations is also discussed. Computer simulations confirm the availability of the proposed approach.

MPM2L-221 -- On the Structure and Performance of Blind Source Separation Based Carrier Phase Synchronization Error Compensation

Ediz Cetin, Izzet Kale, and Richard Morling, *University of Westminster*

A constant need for ever-increasing throughputs through fixed bandwidths has pushed systems designers toward more complex modulation schemes that attempt to achieve the highest possible bandwidth efficiency. This puts stringent constraints on the performance, power efficiency and silicon area of carrier phase synchronisers. In this paper we carry out a detailed performance analysis of the blind-source separation (BSS) based DSP algorithm that tackles the carrier phase synchronisation error problem. The results indicate that the BSS structure can offer adequate performance for most communication systems and lends itself to efficient real-time custom integrated hardware or software implementation

MPM2L-223 -- Biomedical Signal and Image Processing II
Monday: 3:40 pm – 5:00 pm
Chair: Marios Pattichis
University of New Mexico

MPM2L-223 -- A Hierarchical Segmentation Model for the Lung and the Inter-costal Parenchymal Regions of Chest Radiographs

Janakiramanan Ramachandran and Marios Pattichis, *The University of New Mexico*, Peter Soliz and Mark Wilson, *Kestrel Corporation*

A hierarchical image model is used for segmenting chest radiographs. First, we use an Active Shape Model (ASM) to segment the left and right lungs. Then, using the segmented lung, we initialize the segmentation of the inter-costal parenchymal regions, using another four ASM models. We have found that the overall segmentation system is robust, and has been able to adapt to variations in lung height and in the number of inter-costal parenchymal regions.

MPM2L-223 -- Functional Signal detection in Retinal Videos

Eduardo Barriga, *University of New Mexico,* and Peter Soliz, *Kestrel Corporation*

An optical imaging device of retina function (OID-RF) has been constructed to record changes in reflected 700nm light from the fundus caused by retinal activation in response to a visual 535nm stimulus. The objective of this paper is to apply signal detection algorithms that can detect the retinal response following visual stimulation of a region of the retina. We present a statistical analysis of the resulting retinal videos based on non-parametric statistics and hypothesis testing. We compare our results with classification techniques such as using Mahalanobis distance and the nearest neighbor rule.

MPM2L-223 -- Development of Biomedical Imaging Data Analysis and Visualization System - from Molecules to Organs

May Dongmei Wang and Geoffrey Wang, *Georgia Institute of Technology*

In the 21st century, the biggest challenge we are facing is human health. How human body functions on all levels (molecule, cell, organ, whole body), and how diseases (cancers etc.) can be prevented, predicted, or diagnosed early, yet largely remain to be answered. Our lab is working on analysis, modeling, and interactive 3-D visualization of biomedical data at all levels acquired through magnetic or optical imaging techniques. We develop level-of-detail analysis with elliptical weighted average volume splatting to the reconstruct 3-D human body (NLM/NIH Visible Human Project) in VR. We process cancer cell imaging data and build model to visualize molecule functional interactions. The goal is to assist medical professionals in training medical students and in making diagnosis/treatment decisions.

MPM2L-223 -- Heart Rate Variability Characterization Using Correlation Dimension

Xiaobo Miao, Wei He, and Hao Yang, *Chongqing University*, and Heng-Ming Tai, *University of Tulsa*

Heart rate variability (HRV) has become a useful tool for analyzing cardiovascular autonomic control from the electrocardiogram (ECG). Detection and analysis of HRV allows a quantitative and noninvasive method to obtain reliable and reproducible information on autonomic modulation of heart rate. Nonlinear methods (e.g., correlation dimension) are promising tools for HRV assessment. This paper presents a reliable estimation of correlation dimension (D2) for nonlinear HRV analysis. A modified GP correlation algorithm and the selection of parameters are presented. This nonlinear dynamical parameter is then employed for HRV characterization two groups of subjects: healthy subjects and hypertension patients. Results show that D2 in daytime of a healthy person is generally smaller than that at night, whereas the hypertension patients exhibit no specific trend between the D2 in daytime and the D2 at night. The average D2 of hypertension patients after repeated examination two week later decreases (daytime average: 5.89 vs. 5.16; night average: 6.12 vs. 5.81), which implies that treatments possibly function.

MPM2L-225 -- Non-Stationary Signal Processing
Monday: 3:40 pm – 5:00 pm
Chair: Monique Fargues
Naval Postgraduate School

MPM2L-225 -- Automatic Speech/Speaker Recognition in Noisy Environments Using Wavelet Transform

Nadder Hamdy, Waleed Fakhr, and Weaam Alkhaldi, *The Arab Academy for Science and Technology*

Feature extraction represents a crucial step in pattern recognition in general and in speech/speaker recognition in particular. Robustness to most of the common types of noise is essential. This paper presents a Discrete Wavelet Transform- based feature extraction technique for multi-band automatic speech/speaker recognition. Experimental results have shown that this technique is of comparable performance with a full-band (conventional) technique, under matched conditions (clean speech for both training and testing). It has been

found that both techniques are complementary under mismatched conditions (clean speech for training and noisy speech for testing), in that if the features extracted using each of them are combined, better recognition rates are attainable especially at low signal-to-noise ratios.

MPM2L-225 -- Experimental Verification of a Novel Method of Extraction of Nonstationary Sinusoids

Alireza Karimi Ziarani, *Clarkson University*, Ian Morton Blumenfeld and Adalbert Konrad, *University of Toronto*

Experimental verification of the functionality of a novel method of detection, extraction and estimation of amplitude, phase and frequency of sinusoids of time-varying nature is presented. A set of nonlinear differential equations governs the dynamics of the algorithm. The proposed algorithm has been digitally implemented on a digital signal processor (DSP) platform and the laboratory verification of its performance is presented. The algorithm has a very simple structure which renders it suitable for implementation both on hardware and software platforms.

MPM2L-225 -- A Relative Quality Controlled Region-of-Interest Image Coding Based on Wavelet Transform

Shinji Fukuma and Masafumi Ito, *Shimane University*, Chikara Imajo, *Fujitsu Kyushu Digital Technology*, Shotaro Nishimura and Masahiko Nawate, *Shimane University*

A region-of-interesting (ROI) image coding based on wavelet transform that can control the image quality between ROI and region-of-non-interesting (non-ROI) under a constrained quantity of information will be proposed in this paper. We introduce a scalar parameter referred as "beta" to control, and it is ratio of the quality ROI to non-ROI and is relative measure. And a method which can restore the shape information of the region of ROI with few side-information at receive end will be also proposed. Our method can avoid so many information loss for nonROI at lower constrained bit-rate caused in JPEG-2000, maintaining the quality of ROI is higher than non-ROI.

MPM2L-225 -- Wavelet-Based Compression Methods maintaining Multiple Lossless Region of Interest

Monsef Mekouar, Rita Noumeir, and Christian Gargour, *ETS*, and Venkat Ramachandran, *Concordia University*

Images, used in several fields such as medicine or video transmission, contain regions that are more important than others. Compression methods capable of delivering higher reconstruction quality for the important regions are thus attractive. For such cases, only small portions of the image might be essential to the user, and the cost of a wrong interpretation could be high. Methods that deliver lossless compression elsewhere in the image, could be a solution, providing an efficient and accurate image coding. In this paper, we propose two methods, which achieve lossless compression of the regions of interest. Both are based on the embedded zerotree wavelet coding which is used according to two different approaches. In one of these approaches, our method is applied to the whole image, while in the other, it is applied to a subdivision in equal blocks of the image.

MPM2P-140 -- Mixed Signal VLSI
Monday: 3:40 pm – 5:00 pm
Chair: Igor Filanovsky
University of Alberta

MPM2P-140 -- Random Potential Perturbation Effect on a One Dimensional Parabolic Quantum Dot

Hatem El-Matbouly and Mohamed Saleh, *Arab Academy for Science and Technology*, and Motaz Soliman, *Institute of Graduate Studies and Research, Alexandria*

Perturbation treatment of random potential due to the discreteness and smallness of the ions potential in nanoscale devices is presented in this paper. The first and second order correction to the ground, first and second excited states have been calculated using time-independent perturbation theory for an electron confined in a one dimensional parabolic quantum dot. The numerical calculations showed an approximate energy correction of about 1.4 meV due to ion fluctuation potential. In addition the perturbation effect is significant in a dot radius ranging from 60nm to 20nm.

MPM2P-140 -- An Alternative Method for Characterizing Capacitor Matching

Kee-Chee Tiew and Randall Geiger, *Iowa State University*

An alternative method for characterizing capacitor matching is presented. The basic idea of this method is to sense the mismatch among the capacitors by amplifying the error voltage using an iterative switched-capacitor scheme. Through simulation, this method has shown attractive property for sensing capacitor mismatches down to 1% and smaller.

MPM2P-140 -- Offset Removal From Floating Gate Differential Amplifiers And Mixers

Farhan Adil and Paul Hasler, *Georgia Institute of Technology*

A typical differential-pair circuit has an inherent offset between the two input terminals. We show the removal of offsets due to transistor mismatch in circuits based on a differential pair topology, using floating-gate devices at the inputs of the differential pair. This offset will cause non-linearities and second-order distortions in the output. By removing the offsets, we show the output to be very linear over a wide dynamic range, and effectively reduce the second order harmonics for a differential pair circuit. Further analysis is shown for a multiplier cell using the floating gate differential pair. We present an architecture to allow the offset reduction of many multiple differential pair elements via an automatic programming element. This architecture will allow the use of multiple floating-gate differential pairs with minimal time required to program the offset nullification, minimization of I/O pins required for programming, and reduction of complexity and design time in a system.

MPM2P-140 -- MOS-Translinear Morlet Wavelets

Carlos Sanchez-Lopez, Alejandro Diaz-Sanchez, and Esteban Tlelo-Cuautle, *National Institute for Astrophysics, Optics and Electronics*

The design of a low-voltage current-mode Morlet Wavelet, using MOS transistors in weak inversion, is presented. The proposed design is based on two translinear building blocks: a normalized gaussian-function generator and a four-quadrant analog-multiplier. Simulation results using BSIM3.v3 model for a 0.6ƒÝm AMS process parameters, in a CADENCE environment, are presented.

MPM2P-140 -- One Class of Wideband Amplifiers with Monotonic Step Response

Igor Filanovsky, *University of Alberta*

The paper describes the wideband amplifiers that were designed using the first semiperiod of the sin(expk)t function as an approximation of their impulse response. For this class of amplifiers with monotonic step response one can establish a simple relationship between the delay-to-rise-time ratio and the order of transfer

function. Choosing the order one can find the transfer function roots and, hence, to finish the design. To simplify the design the delay-to-rise-time ratio and the transfer function roots are given for the transfer functions from the forth to tenth order. The delay-to-rise-time ratio of the proposed transfer functions is better than that of Bessel or Gaussian filter functions by fifteen to twenty percents.

MPM2P-140 -- Process Dependency of MOSFET Depletion Mode MOS Capacitors in Series Compensation

Wai Yung, Tian Xia, Godi Fischer, and Allen Davis, *University of Rhode Island*

The realization of a linear capacitor using two series connected MOS transistors in depletion mode to compensate for voltage dependence is presented. The capacitance per unit area of is compared to that of a poly-poly and poly metal for several sub-micron processes. The linearity achievable from this technique is predicated for each sub-micron process based on BSIM3 models in HSPICE. There is a significant capacitance over the usable voltage range: 2$W%$ - 10$W%$. Incremental improvements in the linearity are observed as the device geometries are scaled down. In circuits which form ratios of capacitors it is possible for the non-linear errors to match, thereby G-Ratio which is constant over low voltage ranges, despite large changes in capacitance as a function of voltage. Example of switched-capacitor circuits are presented to illustrate where this can be exploited and where it will not work so well. The THD vs. Input signal power is compared in two switched-capacitor circuits.

MPM2P-140 -- Low Voltage Cascode Amplifier

Shahab Ardalan, Kaamran Raahemifar, and Fei Yuan, *Ryerson University*

A 0.8 V folded cascode amplifier was designed in 0.18-?m standard CMOS technology. Emphasis was placed on observing the low voltage design and using current driven bulk (CDB) technique to achieve this goal. The CDB technique was introduced as a method for low voltage design by reducing threshold voltage. This design achieves 141dB DC gain, 56Mhz 3dB band width and 65GHz gain band width, which is the working condition.

MPM2P-140 -- Zeroing on a Zero-temperature Coefficient Point

Igor Filanovsky and Laleh Najafizadeh, *University of Alberta*

The transconductance characteristics of MOS transistors realized in 0.18 mm CMOS technology have a zero-temperature coefficient (ZTC) bias point. The presence of this point influences performance of both analog and digital circuits. The offset voltage drift in a source-coupled differential pair strongly increases, if the transistor drain currents are equal to the bias currents of ZTC point. In this case the drift components of individual transistors are added. It is also shown that it is impossible to find the drain voltage optimizing the temperature stability of propagation delay in digital circuits. One has to divide the digital circuits in two types. In the first type (CPU circuits) the optimal drain voltage is equal to ZTC bias point voltage of n-channel transistors, in the second case (SRAM circuits) the optimal drain voltage is equal to the absolute value of the ZTC bias point voltage of p-channel transistors.

MPM2P-140 -- High Drive Capability Current Summing Amplifier for Audio and Cable Driving Applications

Dattatreya Suryanarayana, *Sanyo LSI Technology India Pvt. Ltd.*

This paper presents current summing amplifier. This circuit consists of Psedo source follower, which uses current summing technique to remove the effect of offset which is a serious problem in psedo source follower. This circuit finds application in driving audio loads of 50 ohms and cables. This circuit is simulated for offset range of 100mv to -100mv. Load is 50 ohms. Signal swing is 0.1v to 3.2v at vdd equal to 3.3v.

MPM2P-140 -- Ultra-Low Constant-Current Generation with MOS Interface-Trap Charge Pump

Ugur Cilingiroglu, *Texas A&M University*, Kenton T. Veeder, *Raytheon*, and Adriana Becker-Gomez, *Texas A&M University*

MOS interface-trap charge pump is explored as a sub-nanoamp constant-current generator. The paper presents an optimized generator structure which can be configured as a current source, current sink or a floating current generator. Rail-to-rail output range, zero temperature coefficient and very high output resistance are demonstrated by experimentation on a test chip. Experimental evaluation of transconductors biased with these configurations are also presented.

MPM2P-140 -- A Very High-Frequency CMOS Self-Biasing Complementary Folded Cascode Differential Difference Current Conveyor with Application Examples

Muhammed A. Ibrahim and Hulusi Kuntman, *Istanbul Technical University*, Oguzhan Cicekoglu, *Bogazici University*

In this paper a very high-frequency CMOS configuration for differential difference current conveyor(DDCC)based on self biasing complementary folded cascode (CFC)circuit is proposed. The circuit uses no additional bias voltage sources other than the two supply rails. In addition, DDCC-based four novel first order all-pass configurations are presented as an example of application of the proposed CMOS DDCC circuit. Simulation results are included to verify the theory.

MPM2P-140 -- Calculation of Amplitude and Frequency in a Current-switching Resonant Oscillator

Igor Filanovsky, *University of Alberta*

The capacitive electrical momentum, Cdv/dt, is an additive quantity, and is convenient tool for the analysis of oscillations in a current switching limit cycle resonant oscillator. The oscillator includes a parallel RLC-circuit driven by a comparator with voltage input and current output (transconductance comparator). The analysis is given for two cases of comparator. In the first case the comparator has an instant switching of current, in the second case the comparator has a finite slew rate of switching. Both the steady-state and transient oscillation amplitude and frequency are calculated. The amplitude transient can be long, if the losses in the parallel circuit are small. The frequency transient is short, and in case of ideal comparator the frequency of steady-state oscillation is settled instantly.

MPM2P-140 -- A Design Path For Optimization-Based Analog Circuit Design

Robert Hägglund, Emil Hjalmarson, and Lars Wanhammar, *Linköping University*

In this paper we describe a design path for optimization-based device sizing of analog circuits. The design path offers an efficient and reliable way to design high-performance analog integrated circuits without the explicit knowledge of an experienced designer. A key feature is that the partial cost functions are generated directly from the circuit topology. To demonstrate the functionality and performance of the approach a folded-cascode operational transconductance amplifier is designed.

MPM2P-140 -- A Programmable Diffuser Circuit Based on Floating-gate Devices

Paul Smith and Paul Hasler, *Georgia Institute of Technology*

This paper presents a programmable diffuser using floating-gate circuits. We present the dynamics of classical diffuser circuits and show the differences between the classical and the programmable case. Programmable diffusers offer many advantages including removing individual element mismatch and also giving the user the ability to reconfigure the overall system behavior. Programmable diffusers can be used for spreading, just as in a resistive network, and they can also be used to create applications based on wave propagation. Experimental data is presented from circuits fabricated on a 0.5μm nwell CMOS process available through MOSIS.

MPM2P-140 -- Design and Use Based on Long-term Measurements of Analog Floating-Gate Array Circuits

Matthew Kucic, Paul Hasler, and Paul Smith, *Georgia Institute of Technology*

Presented are handling and use issues to consider when using floating-gates in analog circuits, such as where to set bias voltages to reduce long-term effects and conditions to avoid when powering up and down the system. Designs to compensate for long-term changes resulting from global disturbances are presented, both for computational blocks as well as bias currents using floating-gates. Also presented is long-term data from an array of floating-gates demonstrating their ability to hold charge over time.

MPM2P-140 -- Simple and Accurate Comparator Circuit

Takeshi Shima and Koujirou Miyoshi, *Kanagawa University*

The novel comparator circuit is proposed. Not only the cross-coupled transistors, but also the load transistors pair block with cross-coupled capacitors contribute to enhance the latch operation. The mechanism is explained in detail. The load circuit of the input differential stage is designed to reduce the input referred offset deviation. The basic idea of this load circuit was proposed in \cite{rui} and the idea is modified to be applicable to the comparator. In this paper, simulated results are shown using VDEC design environment.

MPM2P-140 -- New Parallel Emmitance Simulator Realizations Employing a Single OTRA

Firat Kacar, *Istanbul University*, Ugur Cam, *Dokuz Eylül University*, Oguzhan Cicekoglu, *Bogazici University*, Hakan Kuntman and Ayten Kuntman, *Istanbul Technical University*

In this study, four novel grounded parallel emmitance simulator topologies employing single OTRA are proposed. The presented topologies require fewer passive components than the counterparts in the literature. The performance of the proposed emmittance simulators is demonstrated on a current-mode multifunction filter. PSPICE simulation results are included to verify theory.

MPM2P-140 -- High Performance CMOS Realization of the Third Generation Current Conveyor (CCIII)

Shahram Minaei and Merih Yildiz, *Dogus University*, Hakan Kuntman and Sait Turkoz, *Istanbul Technical University*

In this paper a new CMOS high performance dual-output realization of the third generation current conveyor (CCIII) is presented. The proposed CCIII provides good linearity, high output impedance at port Z and excellent input/output current gain. PSPICE simulation results using MIETEC 1.2m CMOS process model are included to verify the expected values.

MPM2P-140 -- Extraction of Electrical Parameters of Floating Gate Devices for Circuit Analysis, Simulation, and Design

Antonio Mondragon-Torres, *Texas A&M University*, Marcio Cherem Schneider, *Universidade Federal de Santa Catarina*, and Edgar Sanchez-Sinencio, *Texas A&M University*

We propose a structured methodology to extract the electrical parameters of floating gate devices. The characterization of a FG structure requires only two parameters in addition to the conventional MOSFET parameters. This additional set of parameters represents the charge on the FG and the total capacitive coupling of the FG with the control gate. We have characterized the FG device through a comparison of its characteristics with those of a reference transistor. Then we used analytical and simulation MOSFET models in conjunction with the extracted parameters to show the validity of our approach. Our methodology can be applied for the characterization of both flash memories and multiple-input FG devices. Both analytical and simulation models are shown to be in good agreement with experimental results in a 0.35um technology.

MPM2P-140 -- A Comparative Study of Low-Voltage CMOS Current-Mode Circuits For Optical Communications

Fei Yuan, *Ryerson University*, Bendong Sun, *Ryerson Univerisity*

This paper presents a comparative study of the characteristics of low-voltage CMOS current-mode circuits for optical communications. Both the small and large-signal behavior of these circuits are examined. A new low-voltage current-current feedback CMOS current mirror and a new low-voltage pseudo-cascode CMOS current mirror are proposed. These circuits are implemented in a 0.18 μm CMOS technology and analyzed using Spectre. Simulated results demonstrate that the proposed low-voltage CMOS current mirrors offer low input impedance, large output impedance, and large bandwidth. They are particularly attractive for low-cost optical transceiver design.

TAM1L-209 -- Amplifiers III
Tuesday: 9:00 am – 10:20 am
Chair: Mohamad Sawan
École Polytechnique de Montréal

TAM1L-209 -- Use of the Newton-Raphson Iteration to Eliminate Low Frequency Dipoles

Mark Schlarmann and Randall Geiger, *Iowa State University*

Amplifiers with closely-spaced low-frequency pole-zero pairs (dipoles) are normally avoided for applications that require fast and accurate settling because they have slow-settling components in the transient response. In this work, an algorithm that involves a Newton-Raphson iteration is utilized to tune an amplifier with multiple low-frequency dipoles and facilitate their cancellation. The tuned structure is suitable for fast settling applications.

TAM1L-209 -- A High Gain Amplifier Using a Cascading Architecture

Ahmed Hashim, Mezyad Amourah, and Randall Geiger, *Iowa State University*

High gain amplifiers with fast settling times are needed for high-speed data converter applications. Cascading amplifiers is generally a good way to achieve the desired open loop gain however; stability and settling speed become a concern. A cascading architecture that is inherently stable and maintains good settling performance was previously discussed. In this paper, a transistor level three stage implementation is presented that achieves over 100dB of gain while maintaining good settling performance.

TAM1L-209 -- On Synthesis of Wideband Multistage Amplifiers with Monotonic Step Response

Igor Filanovsky, *University of Alberta*, Platon Matkhanov, *SPU*

The paper describes synthesis of the transfer function of the multistage wideband amplifier having a monotonic step response. The procedure is based on approximation of a specially chosen impulse response in the time domain. This target impulse response is constructed using a delayed and exponentially attenuated sinus squared function. The Laplace transform of this pulse is a transcendental function, yet the real and imaginary parts of this transform may be approximated by the polynomials with alternating zeros. The approximation allows one to obtain a realizable transfer function. The design example shows that step response of this transfer function is practically monotonic, and, in addition, has a superior delay-to-rise-time ratio.

TAM1L-209 -- A New Configuration for Current Feedback Operational Amplifiers

Brent Maundy, *University of Calgary*, Peter Aronhime, *University of Louisville*, and Stephan Gift, *University of West Indies*

A new realization of a Current Feedback Amplifier (CFA) is introduced, and a description of its properties is provided. It is shown that this new realization offers several advantages in comparison with conventional CFAs and may be useful in certain design applications. Theoretical derivations are presented, stability issues are examined, and laboratory measurement results are given.

TAM1L-211 -- RF and Microwave Oscillators III

Tuesday: 9:00 am – 10:20 am

Chair: Jose Silva-Martinez

Texas A&M University

TAM1L-211 -- Comparison of Phase Noise Simulation Techniques on a BJT LC Oscillator

Leonard Forbes, Chengwei Zhang, Binglei Zhang, and Iswahyudi Chandra, *Oregon State University*

The phase noise resulting from white and flicker noise in a BJT LC oscillator is investigated. HSPICE, Eldo RF, and Spectre RF simulations of phase noise resulting from the random-phase flicker and white noise in a 2GHz BJT LC oscillator have been performed and demonstrated. The simulation results are compared with the experimental result reported in the literature.

TAM1L-211 -- Genetic Optimization of Charge-Pump PLL Parameters

Giulio Antonini, *University of L'Aquila,* and Fabio Antonini, *Siemens ICN*

The optimal design of a Charge Pump PLL is carried out by means of a Genetic Algorithm. The optimized filter provides a significant reduction of the bandwidth with a limited overshoot. Some tests confirm the proposed approach is able to find a near-optimal solution assuring good performances.

TAM1L-211 -- Differentially Tunable Varactor With Built-In Common-Mode Rejection

Sebastian Magierowski, *University of Toronto,* Krzysztof Iniewski, *PMC-Sierra Inc.*, and Stefan Zukotynski, *University of Toronto*

A circuit-based, differentially tunable MOS varactor with enhanced intrinsic common-mode noise rejection is proposed and analyzed. Using a complementary topology the C-V characteristics of two MOSFETs are arranged to sum under differential excitation and to roughly cancel under common-mode excitation. The benefits of this topology are two-fold: (a) by nature, differential tuning filters common-mode noise and (b) the new structure acts to further reduce common-mode disturbances. Simulations show the effectiveness of this approach against standard techniques. Differential tuning circuits are proposed and alternate varactor structures discussed.

TAM1L-211 -- Comparison of an Inductorless Low-IF and Zero-IF Receiver for Bluetooth

Christian Duerdodt, Andre Hanke, and Stefan Heinen, *Infineon Technologies*, and Ulrich Langmann, *Ruhr-Universität Bochum*

A zero-IF and a low-IF receiver have been implemented in a 0.25um CMOS process to find the best suited receiver architecture for a System-On-a-Chip Bluetooth solution. Due to the on-chip channel select filter both architectures benefit from there high integration level. The simple DC offset compensation and the reduced even-order linearity requirements associated with low-IF receivers contrast with the low power consumption in zero-IF receivers. On-chip coils were avoided to reduce crosstalk and die size in the targeted single-chip solution. The two realized LNA architectures, two mixers, Gm-C and active RC filters have been optimized for the calculated linearity and noise requirements of both receivers. Due to the increased influence of 1/f-noise and higher required linearity in the zero-IF receiver the implemented receivers indicated the better suitability of the low-IF receiver architecture for a CMOS System-On-a-Chip Bluetooth implementation.

TAM1L-213 -- Nyquist Rate Data Conversion I
Tuesday: 9:00 am – 10:20 am
Chair: Won Namgoong
University of Southern California

TAM1L-213 -- A Non-Binary Capacitor Array Calibration Circuit with 22-bit Accuracy in Successive Approximation Analog-to-Digital Converters
Jianhua Gan, *Cirrus Logic/The University of Texas at Austin*, and Jacob Abraham, *The University of Texas at Austin*

A novel capacitor array calibration circuit is presented in this paper. A non-binary capacitor array with 20 capacitors is used. The capacitor calibration algorithm is based on a perceptron learning rule, developed for Artificial Intelligence applications. The capacitor weights are adaptively calibrated to match the physical capacitors with up to 22-bit accuracy. Capacitor matching is not a limiting factor to the resolution. A mixed-signal micro-controller architecture is used to efficiently implement the novel capacitor array calibration algorithm. This calibration circuit is being used to design a 1.5 mega samples per second (MSPS), 16-bit, 50mW successive approximation analog-to-digital converter (ADC).

TAM1L-213 -- An MSB-First Monotonic Switched Capacitor Serial DAC
Mezyad Amourah, Saqib Malik, and Randall Geiger, *Iowa State University*

A monotonic DAC using switched capacitor integrator is presented. For an N-bit digital input sequence, the proposed DAC starts conversion with the MSB and takes N cycles to finish conversion. Some design issues relevant to the design and their possible solutions are also presented

TAM1L-213 -- Design Issues For Low Voltage, High Speed Folding and Interpolating A/D Converters
Ovidiu Carnu and Adrian Leuciuc, *State University of New York*

In this paper are discussed design issues for a folding and interpolating A/D converter (ADC) in 0.35 mm CMOS technology. A new averaging technique is used for reducing the DNL and INL errors. The goal is a speed of 100MS/s and a resolution of 10 bits with a supply voltage of 2.5V or less.

TAM1L-213 -- A Low Power 10 Bit 80 MSPS Pipelined ADC in Digital CMOS Process
Sourja Ray, Preetam Tadeparthy, Shakti Shankar Rath, Dinakaran B. Lavanmoorthy, Sujit C. P. S., and Sumeet Mathur, *Texas Instruments India Ltd.*

This paper describes a 10 bit 80 MSPS low power ADC designed in a 0.18um digital CMOS process for an 802.11a baseband PHY chip. The receive channel in the AFE consists of dual ADCs used to digitize the I & Q channels in a direct conversion receiver. Novel features in this design includes a 6-bit offset cancellation DAC integrated in the S/H and a amplifier sharing topology that help in reducing overall power and area. Low power is achieved through the use of the digital supply (1.8V) provided to the chip which allows the fastest digital core transistors to be used in the design without reliability issues and also makes the design suitable for integration with the digital baseband section. Each ADC consumes less than 60mW of analog power including the reference and about 20mW of switching power. The device is designed for -62dB THD performance and 58dB SNR for an 11MHz signal band making it among the lowest power ADCs in its class described in literature.

TAM1L-214 -- IP, Embedded Cores, and Systems on a Chip I

Tuesday: 9:00 am – 10:20 am

Chair: Wael Badawy

University of Calgary

TAM1L-214 -- Empirical Performance Estimation of IFFT/FFT Cores for OFDM Systems-on-a-Chip

Kostas Pagiamtzis and Glenn Gulak, *University of Toronto*

Quick and accurate estimation of area, speed, and power of IP cores for SoC implementations can help reduce design time and thus the overall cost. Accurate performance estimation early in the design cycle is valuable for identifying trade-offs in the different blocks that make up an SoC. This work provides an empirical estimation method for IFFT/FFT blocks in multicarrier or OFDM systems that was verified through the design of a 0.18 µm CMOS test chip. The methodology inefficiency factor (MIF) is introduced as metric for evaluating the area efficiency of a digital design flow.

TAM1L-214 -- Variable-Rate Pipelined Multiplier Design for Reconfigurable DSP Applications

Sangjin Hong and Shu-Shin Chin, *SUNY at Stony Brook*

This paper presents a VLSI design and implementation of a variable-rate multiply-and-accumulate (MAC) block for DSP applications. The pipeline depth of the multiplier is dynamically controlled given the throughput requirement of the application. The depth of pipeline varies at the hardware level which controls the rate of execution to save power consumption. The MAC is targeted for a coarse grain FPGA design to support a wide range of digital signal processing applications. The power consumption is lowered by reducing the unnecessary register switching. The technique is applied to carry-save and Booth recoded multipliers. The MAC circuit is designed in 0.35-micron CMOS processing technology and evaluated for current DSP applications.

TAM1L-214 -- MPEG-4 Synthetic Video Object Prediction Using Embedded Memory

Mohammed Sayed and Wael Badawy, *University of Calgary*

Synthetic video object tools in MPEG-4 use a mesh topology representation that expresses the dynamic of the video object using motion of control points (i.e. nodes). It uses affine transformation to predict the video object from the deformation of the mesh topology. This paper presents SIMD (single instruction stream multiple data stream) architecture that prototypes an embedded memory for video motion compensation using affine transformation as defined by MPEG-4. The affine transformation computations are distributed on the parallel processing elements to improve the performance and reduce the power consumption. In addition, the embedded memory is optimized to be suitable with the parallel implementation. The proposed architecture is prototyped, simulated and synthesized for 0.18 mm CMOS technology using TSMC standard cells.

TAM1L-214 -- A Prototype of WideBand/Ethernet Bridge using WEMAC

Omar Elkeelany and Ghulam Chaudhry, *University of Missouri-Kansas City,*

In this paper we present a full System prototype for the WideBand/Ethernet Bridge for Application Specific Integrated Circuit, (ASIC) Using WEMAC. WEMAC is the WideBand Embedded Media Access Controller (WEMAC), which provide the efficient bandwidth for WideBand network users. WEMAC controls the flow of data between its different network devices. WEMAC prevents collisions using the Buffered Packet Synchronization (BPS) approach. It also eliminates the need of a computer to connect any digital device to a Local Area Network (LAN), with significant improvement for the performance/cost ratio. WEMAC is synthesized in FPGA using ASIC. Performance characteristics like power consumption and delay are measured using the ASIC tool. Analysis reveled that WEMAC reduces the power consumption. If the devices are no longer consuming high power, they can be powered through a category-5 network cable and eliminate the process of

regular electrical power outlet installations and maintenance. The full System prototype can be used in future for quantitative buffer measures, and total performance/cost evaluation.

TAM1L-216 -- VLSI Routing, Partitioning and Placement

Tuesday: 9:00 am – 10:20 am

Chair: Robert Reese

Mississippi State University

TAM1L-216 -- Congestion Based Mathematical Programming Models for Global Routing

Laleh Behjat, Anthoni Vannelli, and Andrew Kennings, *University of Waterloo*

Global routing is an essential part of physical design. Global routing has been traditionally formulated to minimize either the total wirelength or the maximum channel capacity of a circuit ignoring important issues such as congestion and number of bends. In this paper, a mathematical programming model, which is capable of incorporating different aspects of the global routing problem, such as wirelength, maximum capacity, number of bends in each route and congestion is presented. The main advantage of this model is its flexibility to deal with different aspects of the routing. Our congestion estimation gives lower and upper bounds on the maximum number of wires passing through each channel. The global routing problem is solved as a relaxed linear programming problem using interior point techniques. Experiments on different benchmarks show that the new model builds a flexible and powerful technique which enhances the global routing solution.

TAM1L-216 -- Octilinear Steiner Tree Construction

Charles Chiang, *Synopsys, Inc.,* and Ching-Shoei Chiang, *Soochow University, Taiwan, ROC*

We propose a linear time algorithm to convert a existing rectlinear Steiner tree to an isomorphic octilinear Steiner tree with reducing total wirelength. We prove the total wirelength of octilinear Steiner tree obtained by our algorithm is the lower bound. We also run 15 designs to find an average 6.63% wirelength reduction.

TAM1L-216 -- Detailed Routing in a Hierarchical CPLD

Andrew Kennings and Laleh Bedhat, *University of Waterloo,* and Alan Coppola, *Cypress Semiconductor Corporation*

We describe the detailed routing of a commercial Complex Programmable Logic Device (CPLD). The hierarchical, course-grained architecture of the CPLD lends itself to a novel hybrid router that combines a negotiated maze-router with a flow-based router. Numerical results illustrate that our router is significantly faster than a flat maze-router. It also has a higher completion rate compared to a commercial router while producing routings of comparable quality.

TAM1L-216 -- Channel Height Estimation in VLSI Design

Lun Li and Theodore Manikas, *University of Tulsa,* and He Jin, *Oklahoma State University*

This paper presents four methods to estimate channel height for congestion analysis in VLSI design automation. Our channel height estimation methods consider constraint graphs and net types in a channel. The experimental results show that the proposed methods yield better results than existing methods.

TAM1L-218 -- Ad Hoc Networks
Tuesday: 9:00 am – 10:20 am
Chair: Mingyan Liu
University of Michigan

TAM1L-218 -- Energy Efficiency in Many-to-One Communications in Wireless Networks
Enrique Duarte-Melo and Mingyan Liu, *University of Michigan*

This paper analyzes the energy consumption in a wireless network where communication occurs in a many-to-one fashion. We consider both a multi-hop transmission and using clusters. When using clusters, the transmissions within the cluster use multiple hops, and the transmission from the cluster head to the final receiver is done in a single hop. Two factors affect the energy consumption the most. One is the range of transmission used. Clearly the bigger the range the more energy the node needs to transmit successfully. On the other hand in many-to-one communications the throughput can be improved with an increased range of transmission. The improvement in the throughput reduces the energy spent transmitting a given amount of data. The second factor is the number of clusters used, which may vary from 0 (multi-hop alone) to n (every node is a cluster head which reduces to single-hop). This also affects throughput and has an effect on the energy needed to transmit a given amount of data. We show how to balance the effect of these factors to obtain the network organization that minimizes energy consumption.

TAM1L-218 -- Security in IP-based Ad hoc Networks
Rajesh Talpade and Anthony Mcauley, *Telcordia Technologies*

The unique end-to-end communication capability provided by the Internet Protocol (IP) has resulted in ad hoc networks increasingly relying on the IP protocol stack. The same seamless connectivity afforded by IP also renders it easy for malicious users to launch various attacks on ad hoc networks. While numerous approaches have been suggested for addressing security issues, not much standardization work has emerged. We survey the most promising approaches, and discuss ad hoc network security standardization issues in this paper.

TAM1L-218 -- Protocols for Local Data Delivery in Wireless Microsensor Networks
Wendi Heinzelman, *University of Rochester,* Nael Abu-Ghazaleh, *SUNY Binghamton,* Zhao Cheng, Mark Perillo, and Bulent Tavli, *University of Rochester,* and Sameer Tilak, *SUNY Binghamton*

Sensor networks are becoming increasingly important as tools for monitoring remote environments. As sensors are typically battery-operated, it is important to efficiently use the limited energy of the nodes to extend the lifetime of the sensor network. Two factors can greatly influence the performance of protocols for these networks-- the data delivery model, which describes how the end user wants to access the data, and the network dynamics, which include sensor mobility as well as changes in sensor data rates throughout the lifetime of the network. In this paper, we look at several media access control protocols for sending data from sensors to a local data collector. Comparing these protocols shows that there is an inherent tradeoff in energy efficiency with adaptability of the protocol.

TAM1L-218 -- Performance Analysis of WMPLS Signaling and Control in Ad Hoc Networks
Sang-Chul Kim, Kannan Srinivasan, Mauricio A. Subieta Benito, and Jong-Moon Chung, *Oklahoma State University*

The framework of wireless multiprotocol label switching (WMPLS) technology in applications of ad hoc networking and mobile ad-hoc networking (MANET) are presented in this paper. WMPLS has been designed to be a homogeneous protocol to MPLS, GMPLS, and MPLambdaS, which are the strongest candidates for next generation WAN technologies. This paper provides the framework of WMPLS and its signaling/control protocols to establish connection-oriented and connectionless label switched paths (LSPs) in mobile communication

networks and ad hoc networks, and also provides a performance analysis compared to other wireless technologies.

TAM1L-219 -- Neural Networks for Filtering and Instrumentation

Tuesday: 9:00 am – 10:20 am
Chair: Roger Schultz
Halliburton Company

TAM1L-219 -- A Neural Network Based Data Association Technique for Tracking

Mohamad Farooq, *Royal Military College of Canada,* and Thomas Robb, *DND (Canada)*

In tracking, the origin of measurements is usually uncertain due to random interferences. To overcome this problem, a data association technique is required to associate each measurement with the appropriate target or to discard it as arising from clutter or false alarm. In this paper, a neural network approach based on a Hopfield network is presented. The simulation results are compared with the conventional methods based on the Bayesian technique.

TAM1L-219 -- The Use of Differential Evolution to Determine Globally Optimal Connection Weights for Artificial Neural Networks

Mark Buckner, *Oak Ridge National Laboratory*

The goal of any artificial neural network training approach is determination of optimal connection weights. The most widely used approaches are based on variations of gradient-descent techniques and are know to be susceptible to getting trapped in local minima. Differential Evolution (DE), a population based direct search method, has recently been shown to effective at solving real-world multi-objective optimization problems. This paper presents the use of DE to determine globally optimal connection weights. The results obtained with DE will be compared to a backpropagation approach to demonstrate the promising capabilities of DE.

TAM1L-219 -- Efficient Information-Theoretic Model Input Selection

Paul Deignan, *Purdue University*

Of fundamental importance to proper system identification and virtual sensing is the computational determination and assessment of an optimal set of input signals independent of the final model form. If the system is causal and deterministic, it is possible to efficiently compute an information-theoretic optimal input set for a desired uniform accuracy of the target estimate and maximal dimension of the candidate input set. To this end, this paper presents a coherent methodology.

TAM1L-219 -- Neural Networks applied to Automatic Fault Detection

Stefan Jakubek and Thomas Strasser, *Vienna University of Technology*

In this paper a fault detection scheme for engine test-beds is presented. The detection scheme has to process up to several hundreds of different measurements at a time and check them for consistency. The main problem lies in the fact that besides the available data no further information is provided. Our fault detection scheme works as follows: First, principal component analysis of training data is used to determine nonsparse areas of the measurement space. This step is absolutely necessary in order to compress information and thus reduce the number of inputs to the neural network. Since no information about functional relationships between data channels are known a-priori, a statistical approach was chosen. The distribution function of the available data is estimated using kernel regression techniques. Fault detection is accomplished by checking whether a new data record lies in a cluster of training data or not. Areas or clusters for valid data are determined through kernel regression. In order to reduce the computational effort the distribution functions are approximated by neural networks. In order to use as few basis functions as possible a new training algorithm for ellipsoidal basis function networks is presented. The training algorithm works completely autonomous: Both the center locations

and the number of neurons are determined without any supervision. The spread-parameter matrix of every neuron is computed such that data points in the vicinity of the neuron's center are approximated up to the second order. Thus the number of neurons can be reduced drastically. Since even during normal operation of the engine test-bed new training data are provided for fault detection, the system must be able to update itself recursively. For this purpose algorithms both for recursive PCA and for recursive network training are presented. Application to measured data from a real automotive process show that the proposed algorithm yields good results.

TAM1L-221 -- Special Purpose Filter Designs

Tuesday: 9:00 am – 10:20 am

Chair: Domenic Ho

University of Missouri

TAM1L-221 -- Design and Implementation of IS-95 CDMA Baseband Filter

Jianghong Yu and Yong Lian, *National University of Singapore*

A VLSI implementation of pulse-shaping filter for IS-95 Code Division Multiple Access (CDMA) systems is presented. The original IS-95 48-tap pulse-shaping FIR filter is designed using a computational efficient filter structure based on prefilter-equalizer technique. It is shown that the new structure not only achieves 37% savings in the number of multipliers, but also reduces the word length of the coefficients when applied to IS-95 CDMA baseband filter. The VLSI implementation shows that the new structure reduces the chip area and power consumption considerably compared with the direct-form implementation.

TAM1L-221 -- One Structure for a Multistage Running-Sum Decimation Filter

Gordana Jovanovic-Dolecek and Sanjit K. Mitra, *University of California Santa Barbara*

This paper presents a new running-sum decimator for an even decimation factor. The decimator is designed as a cascade of an integrator and a differentiator making it possible to move the integrator section to a lower rate, which is the half of the high input rate. The structure consists of three main sections: a cascade of the first-order moving average filters, a cascade of integrators and a cascade of differentiators. With the aid of the polyphase decomposition, the polyphase components of the first section can be operated at still lower rate.

TAM1L-221 -- Low Power Sigma Delta Decimation Filter

Shailesh Nerurkar, Khalid Abed, Raymond Siferd and Vivek Venugopal, *Wright State University*

This paper presents an efficient design and implementation of a low power digital decimation filter. We implement a low power decimation filter with a narrow transition Finite Impulse Response (FIR) filter using Canonic Signed Digit number (CSD) system. We use multi-stage multi-rate signal processing to design and implement half-band filters and narrow transition band FIR filters. The decimation filter is designed using Simulink, DSP Blockset and simulated using MATLAB. The FIR filter has been coded in Verilog and implemented using FPGA Xilinx 4000 technology. The power consumption of the proposed decimation filter is reduced by 67% compared to the conventional 4-stage Comb-FIR architecture.

TAM1L-221 -- The Design of a Digital Filter for Noise Reduction in an Encoded Speech Signal

Yunhong Li and K. C. Ho, *University of Missouri-Columbia*, Tong Wang, *Motorola*

Coding/decoding of noisy speech introduces correlation between speech and noise, which makes the conventional Wiener filter derived from the decoded signal inefficient for noise reduction. This paper proposes a filter design method by using the linear prediction coefficients from the encoded speech data to reduce noise in an encoded speech signal. The proposed design method reduces the correlation between speech and noise, which provides better quality on the enhanced speech signal.

TAM1L-223 -- Multi-Media and Content Based Retrieval
Tuesday: 9:00 am – 10:20 am
Chair: Dipti Prasad Mukherjee
University of Virginia

TAM1L-223 -- A Qualitative Examination of Content-Based Image Retrieval Behavior using Systematically Modified Test Images
J.C. French, W. Martin, and J.V.S. Watson, *University of Virginia*

We describe the outcome of an effort to understand the behavior of content-based image retrieval (CBIR) technology by examining the behavior of a CBIR system in response to carefully constructed input query images. This work is preliminary and only considers a single CBIR system, Simplicity. We chose this particular system for expediency. It is our intention to develop a methodology suitable for examining any CBIR system.

TAM1L-223 -- Web Query Reformulation by Knowledgeable Agents
Sandip Sen, Sabyasachi Saha, and Partha Sarathi Dutta, *University of Tulsa*

Personal agents have been developed that assist user with information processing needs by generating, filtering, collecting, or transforming information. On the other hand internet stores are providing services customized by the needs and interests of individual customers. Such services can be viewed as ``seller's agents" whose goal is to push merchandise and/or services on to the users. This leads us to believe that there is a growing need for deploying ``buyer's agents" whose goal is to best serve the consumer's interests. We have identified several key functionalities of such buyer's agents: informing consumers of complex interactions between specified preferences and prevailing market conditions, providing differential analysis for decision support, using domain ontologies to help the user reformulate in queries. In this paper, we present a prototype buyer's agent that demonstrate some of these functionalities in a an apartment locator domain.

TAM1L-223 -- Agent based Peer to Peer Systems
Prithviraj Dasgupta, *University of Nebraska*

With the rapid increase in the number of users accessing the Internet over the last few years, Web-servers on different online sites are deluged with client requests. With the increasing demand for Web-based services the client-server paradigm is being replaced by the peer-to-peer paradigm where clients interact with each other for real-time collaboration and information sharing in a large-scale environment. The immense popularity of services such as Gnutella, Napster, and SETI@home indicate that Internet users are comfortable with adapting to the peer-to-peer computing paradigm. The peer-to-peer model offers several design and implementation challenges. A node in a peer-to-peer network needs appropriate techniques for determining peers that possesses useful resources, algorithms for trading those resources between the peers and a trust model for sharing resources. On the other hand, they also need to address economic issues such as incentives to clients that share their resources with peers and preventing free-riders from exploiting the system. Most of the current peer-to-peer systems employ message-based communication to facilitate the interaction between peers. In this paper, we discuss the important issues related to resource sharing on a network of peer machines using software agents.

TAM1L-223 -- Retrieving Similar Images In Image Database Using Relational Matrix
Dipti Mukherjee and Scott Acton, *University of Virginia*

Retrieving similar images in an image database is a challenging problem in CBIR. The definition of perceptual similarity between two images is a function of distance between image features, for example, shape, color and texture features of dominant image regions. We propose a relational matrix based distance measure that can be used effectively to measure similarity between images in a given image database. An Individual relational matrix describes the spatial and functional relations between neighboring image segments in the 2D image matrix. The shape and color features based similarity between neighboring segments are stored in the relational matrix. We have already shown that agglomerative clustering technique is an efficient tool for image segmentation without

having any a priori knowledge of possible number of clusters present in the image. After successful image segmentation, the agglomerative clustering generates a powerful relational matrix describing the major image regions and their spatial and functional relations. To measure similarity between two images, therefore, we need a distance measure between corresponding relational matrices representing those two images. In this paper, this segmentation generating relational matrix is extended and integrated for the purpose of image matching and retrieval.

TAM1L-225 -- Power Systems I

Tuesday: 9:00 am – 10:20 am

Chair: Philip Yoon

University of Oklahoma

TAM1L-225 -- Power System Stability Analysis Using Cell to Cell Mapping

Gautam Patel and Kaveh Ashenayi, *The University of Tulsa*

Cell mapping is a powerful mathematical tool that is employed in the study of dynamical system. Synchronous generators used in power systems are dynamical systems and have a transient behavior. This paper describes cell mapping in brief and presents its application in synchronous generator stability analysis, especially transient stability. Cell maps are used to analyze the global behavior of the synchronous generators. This paper also introduces the use of matrices to make comparisons between two cell maps.

TAM1L-225 -- Application of Virtual Instrumentation in a Power Engineering Laboratory

Qamar Arsalan, Amanda Filbeck, and Thomas Gedra, *Oklahoma State University*

This paper presents a few of the OSU-Stillwater Power Engineering Laboratory capabilities. Digital signal acquisition and virtual instrumentation (National Instruments' LabView software) are used to help students understand the concepts by visualizing the data. Some features of virtual instrumentation are real-time display of waveforms, phasor diagrams, real and reactive power, spectral analysis as well as the ability to interpret the data graphically. Some techniques for improved laboratory practice as well as the laboratory capabilities concerning experiments of transformers and rotating machines are presented.

TAM1L-225 -- Estimation of UPFC Value using Sensitivity Analysis

Seungwon An and Thomas Gedra, *Oklahoma State University*

This paper presents an estimation technique to obtain a value of the unified power flow controller (UPFC) using sensitivity analysis. Modeling of the UPFC inserted in a transmission line is presented for use in an optimal power flow (OPF). An efficient technique to obtain the first- and second-order sensitivities of the generation cost with respect to UPFC control parameters, are described. A case which shows the limitations of our sensitivity method is also analyzed.

TAM1L-225 -- Eigenvalue and Eigenvector Sensitivities Applied to Power System Steady-State Operating Point

John Condren and Thomas Gedra, *Oklahoma State University*

This paper proposes techniques used in finding a power system operating point that is both economically optimal and stable in the small-signal sense. To make the system small-signal stable, we should choose a power system operating point such that changes in system state variables due to small disturbances die out quickly. Thus, we need to know how changes in the power system operating point affect the linearized system's eigenvalues, i.e. the eigenvalue sensitivities. Methods to compute eigenvalue and eigenvector sensitivities are discussed.

TAM1P-140 -- High Performance Digital Circuits and VLSI Design Methodologies
Tuesday: 9:00 am – 10:20 am
Chair: Cristian Chitu
UCLA

TAM1P-140 -- Capacitor Coupling Threshold Logic

Cheng Jia and Linda Milor, *Georgia Institute of Technology,* and Hong-Yi Huang, *Fu-Jen University*

A novel high-speed dynamic CMOS capacitor coupling threshold logic(CCTL) family is proposed in this paper. In the proposed logic family, all the input signals are coupled to one transistor gate of a differential transistor pair through coupling capacitors. A reference signal is coupled to the other transistor gate of the transistor pair. The voltage difference between these two gates is amplified by a sense amplifier to generate two complementary logic outputs. For CCTL gates with a large number of inputs, the transistor count, interconnections and parasitic capacitances in the signal path are reduced significantly, which results in high switching speed and small chip area. Furthermore, there is no DC power dissipation in CCTL gates. Additionally, a CCTL gate is able to provide two complementary logic outputs at the same time, making CCTL suitable for easy implementation of complex logic functions. CCTL can be fabricated with a standard double-polysilicon CMOS process. This paper presents design examples of typical CCTL gates, which have been simulated with 0.18 um TSMC process models to demonstrate superior switching speed compared to static CMOS and Domino logic at the expense of slightly higher dynamic power dissipation.

TAM1P-140 -- A Leakage Tolerant Energy Efficient Wide Domino Circuit Technique

Mohamed Elgebaly and Manoj Sachdev, *University of Waterloo*

Deep submicron noise, especially leakage current, greatly impacts the performance of wide dynamic gates. Quite often, energy is traded off for increased leakage tolerance. In this paper, a leakage tolerant energy efficient wide domino gate is presented. The proposed technique achieves faster evaluation by splitting the wide gate into two sections and consequently slashing the capacitance of the dynamic node by half. Using the new technique, the same level of leakage tolerance can be achieved with around 12% and 28% reduction in energy for 16-input and 32-input OR gates, respectively, compared to the conventional technique.

TAM1P-140 -- Providing a Complete Solution to an Engineering Problem with a Student-Based Academic Project

Justin Ford and Carl Latino, *Oklahoma State University*

A major and important part of engineering education is engaging in projects that are similar to real world engineering problems. The project served the purpose of fulfilling the customer's needs as well as providing a challenging scholastic exercise for students. The project was completed by a student working in conjunction with a faculty member and the result of the project is a solution that satisfies the requirements of the customer. The purpose of this paper is to describe the process by which a student project can reach a full, successful completion in an academic environment.

TAM1P-140 -- Single-Rail Self-timed Logic Circuits in Synchronous Designs

Frank Grassert and Dirk Timmermann, *University of Rostock*

This paper presents a self-timed scheme for dynamic single-rail logic integrated in a single phase clock design. A generalized completion detection for generation of self-timed signals from single-rail gates is described and we show a novel application of the redundancy of a SD-adder to ease the self-timed signal generation. Further we discuss an universal evaluation scheme to overcome the problem of only non-inverting functions with dynamic single-rail gates. The presented SD-adder was integrated in a synchronous scheme and combines the advantages of simple synthesis and clock distribution for synchronous designs with fastest evaluation. Self-timed schemes result in fastest latch-free structures and robustness against clock-skew. Further the single-rail scheme on gate-level yields lower power consumption and smaller circuits. The use of inverting and non-inverting

single-rail gates makes the synthesis close to standard synthesis. Simulations for the redundant adder design show area and power savings of 40% and 30% compared to complementary DOMINO logic structure.

TAM1P-140 -- A Low Power and Reduced Area Carry Select Adder

Kuldeep Rawat, Tarek Darwish, and Magdy Bayoumi, *University of Louisiana at Lafayette*

A carry select adder (CSA) can be implemented by using single adder block and an add-one circuit instead of using dual adder blocks. The add-one circuit is based on "first" zero detection logic and few multiplexers. In modified CSA, one of the n-bit adder blocks is replaced by an add-one circuit consisting of fewer transistors. This scheme considerably reduces the power and area with negligible speed penalty. For 8-bit length n = 8, this modified CSA requires 38% fewer transistors and consumes only 73% of power compared to conventional design using a 0.5- micron CMOS technology.

TAM1P-140 -- High-performance Divider Using Redundant Binary Representation

Guoping Wang, Murad Ozaydin, and Monte Tull, *University of Oklahoma*

A high-performance iterative divider circuit using a previously developed redundant binary inner-product processor core is investigated in this paper. The intermediate quotient coefficients are kept in Redundant Binary (RB) form without converting back to 2's-complement numbers. A unified multiplier using redundant binary representation for both signed and unsigned numbers is investigated. Goldschmidt and Newton-Raphson division methods are compared and the equivalence of these two methods is provided.

TAM1P-140 -- Switching Activity Modeling of Multi-rail Speed-independent Circuits - A Probabilistic Approach

Jia Di and JiannShun Yuan, *University of Central Florida,* Michael Hagedorn, *Theseus Logic Inc.*

A novel switching activity modeling method for multi-rail speed-independent circuits is presented. Based on a newly defined term, Occurrence Probability, plus a simple correlation-modeling algorithm, this method is able to calculate switching activity at each node. The results are verified by Synopsys simulation. Very good agreement between the theoretical predictions and simulation results is obtained.

TAM1P-140 -- An Optimal Variable Voltage Scheduling

Songtao Huang, Chunhong Chen, and Majid Ahmadi, *University of Windsor*

With the development of mobile and portable appliances, there is a strong need for reducing the energy in integrated circuit chips. Dynamic voltage scaling (DVS) techniques reduce energy consumption by changing the operating speed and voltage at real-time based on the workload of the operation. In this paper, we address the optimal variable voltage scheduling problem for different workloads to save the maximum energy. Both static DVS and real-time DVS methods are investigated.

TAM1P-140 -- A Compact Software-Controlled Clock For SoC Application

Pao Chen and Chen-Yi Lee, *National Chiao Tung University*

A compact software-controlled clock multiplier for SoC application is presented in this paper. The control mechanism of clock multiplier includes frequency acquisition, phase acquisition and phase/frequency maintenance modes. These operations sequence are programmable. Our proposed clock multiplier is integrated with an 8-bit microcontroller in order to verify the proposed software-controlled mechanism.

TAM1P-140 -- A New Ternary MVL Based Completion Detection Method for the Design of Self-Timed Circuits Using Dynamic CMOS Logic

Christopher Connell and Poras Balsara, *The University of Texas at Dallas*

The performance and success of many self-timed design methodologies commonly rely heavily on completion detection schemes in order to reliably acknowledge the termination of a computation associated with a self-

timed functional block. A particularly vexing problem associated with many self-timed completion detection schemes proposed in the literature, is the task of implementing the robust and successful generation of a completion done signal, denoting the termination of a self-timed event, on every computation handled by a self-timed functional block. Many research groups who have focused on the development of asynchronous self-timed design methodologies have proposed methods to successfully detect the completion of a self-timed computation. However, a universally acceptable solution that successfully detects the completion of a self-timed event on every cycle of computation for an arbitrary self-timed functional block, remains to this day, an elusive technical issue. In this paper, the authors' propose a novel approach to completion detection, for use in asynchronous self-timed designs, that employs a ternary multiple valued logic ("MVL") approach using dynamic CMOS circuit design techniques, that guarantees the fail-proof generation of event termination on every self-timed computational cycle.

TAM1P-140 -- A Hardware Implementation in FPGA of the Rijndael Algorithm

Cristian Chitu and Frank Chang, *University of California, Los Angeles*

Implementation in FPGA of the new Advanced Encryption Standard, Rijndael, was developed and experimentally tested using the Insight Development Kit board, based on Xilinx Virtex II XC2V1000-4 device. The experimental clock frequency was equal to 75 MHz and translates to the throughputs of 739 Mbit/s for Rijndael with block size and key size of 128 bits, respectively. This circuit has capability to handle encryption/decryption and fitted in one FPGA taking approximately 84 % of the area. The pipelined architecture of our circuit allows to process the data in parallel with encryption or decryption.

TAM1P-140 -- A Parallel Algorithm for Power Estimation at Gate Level

Mehrdad Nourani and Shahin Nazarian, *The University of Texas at Dallas*

In this paper we present an analytical method for estimating switching probability and power consumption of combinational circuits at the gate level. Considering the signal correlation and multiple-bit input switching, we propose an efficient scheme to estimate switching probability and dynamic power consumption of combinational CMOS circuits at the gate level accurately. Additionally, our algorithm has potential not to propagate the estimated values through the circuit and thus can be run in parallel machines for very large circuits.

TAM1P-140 -- Scaling of Serially-connected MOS Transistors with Constant Area Constraint

Ahmed Elkammar, *City College of New York*, and Srinivasa Vemuru, *Ohio Northern University*

Transistor channel width tapering in serially connected MOSFET chains decreases propagation delay and falling times, and reduces the power dissipation. Tapering is the process of changing the size of each transistor width within the serial chain, such that the largest transistor is connected to the power supply rail and the smallest transistor is connected to the output node. Analytical approaches are used to determine the optimal tapering factor for the serially connected MOSFET chain. Under the constant area constraint, the area gained from unscaled transistor widths is reallocated to the transistors using empirical approaches such that the overall delay is improved.

TAM1P-140 -- Quick Memory Stream Locality Analysis

Juha Alakarhu and Jarkko Niittylahti, *Tampere University of Technology*

Profiling a memory stream and a memory system will have an increasing importance in the future as memory systems are getting more complex and the gap between processor and memory speeds increases. This paper proposes simple numerical metrics for measuring both temporal and spatial locality. The developed metrics make a strong simplification of a complex issue, but they provide a convenient method to study and distribute information about locality. To facilitate applying the metrics, a tool capable of calculating them is presented. Finally, the metrics and the tool are demonstrated by examining the locality of the post-cache access stream. The results show how the cache decreases the temporal locality of the memory stream, but the spatial locality does not behave as consistently.

TAM1P-140 -- Minimizing the Number of Registers and the Number Phases in Synchronous Digital Designs with Minimal Clock Period

Noureddine Chabini, *Université de Montréal*

Methods based on modulo scheduling for software pipelining have been recently proposed to minimize the clock period of synchronous digital designs. These methods can be framed in the following four-steps process: in Step 1, the minimal clock period P has to be determined; in Step 2, a valid periodic schedule of the computational elements is computed; in Step 3, registers are inserted in the circuit according to the computed schedule; in Step 4, phases to control registers are determined. In this process, the challenge is how to realize the steps 2, 3 and 4 in order to minimize the number of registers and the number of phases. In this paper, we address the problem of computing a valid periodic schedule of the computational elements, and placing registers while minimizing the number of registers and the number of phases. We propose a mathematical formulation to this problem, and a mixed integer linear program to solve it. We present preliminary experimental results to show the effectiveness of the proposed approach.

TAM1P-140 -- Lorenz Chaotic Model Using Filed Programmable Gate Array (FPGA)

Mohammed Aseeri, *University of Kent at Canterbury*

In this paper, we introduce a new method to implement chaotic generators based on Lorenz chaotic system given by the state equations by using Filed Programmable Gate Array (FPGA). The aim of this method is to increase the frequency of the chaotic signals. The new method is based on MATLAB® Software, Xilinx System Generator, Xilinx Alliance tools, Leonardo spectrum or Synplicity Synplify and ModelSim XE PLUSE. The toolbox of the Xilinx System Generator used as toolbox under MATLAB® Simulink toolbox to convert any MATLAB® Simulink model to the Xilinx System Generator model then to generate the VHDL code for that model. The hardware can be used directly in chaotic communication systems with high frequency.

TAM1P-140 -- On the Information Engine of Circuit Design

Denis Popel, *Baker University,* and Nawar Al Hakeem, *University of Wollongong*

This paper addresses a new approach to find a spectrum of information measures for the process of digital circuit synthesis. We consider the problem from the information engine point of view. The circuit synthesis as a whole and different steps of the design process (an example of decision diagram is given) are presented via such measurements as entropy, logical work and information vitality. We also introduce new information measures to provide better estimates of synthesis criteria. We show that the basic properties of information engine, such as the conservation law of information flow and the equilibrium law of information can be formulated.

TAM2L-209 -- Current Amplifiers
Tuesday: 10:40 am – 12:00 pm
Chair: Mohamad Sawan
École Polytechnique de Montréal

TAM2L-209 -- Comparison of New and Conventional Low Voltage Current Mirrors
Francisco Ledesma, *New Mexico State University,* Rafael Garcia, *Delphi Automotive Systems,* and Jaime Ramirez-Angulo, *New Mexico State University*

A comparison of several new architectures of low voltage high performance CMOS current mirrors is presented. The comparison includes: Input impedance, output impedance, gain accuracy, frequency response and input and output voltage requirements Experimental results of a test chip prototype are shown that are in good agreement with theoretical predictions.

TAM2L-209 -- A Low-Voltage MOS Cascode Current Mirror for All Current Levels
Bradley Minch, *Cornell University*

In this paper, we describe a simple low-voltage MOS cascode current mirror that functions well at all current levels, ranging from weak inversion to strong inversion. The circuit features a wide output voltage swing and requires an input voltage of approximately one diode drop plus a saturation voltage. We present experimental results from a version of the current mirror that was fabricated in a 0.5-um CMOS process along with a comparison with several other current mirrors with respect both to required input voltage and to output compliance voltage.

TAM2L-209 -- A New Low-Voltage Fully-Balanced Wide-Band Differential CMOS Current Amplifier
Bendong Sun and Fei Yuan, *Ryerson University*

This paper presents a new low-voltage fully balanced wide-band differential CMOS current amplifier. The number of transistors between the power and ground rails is minimum so that the minimum supply voltage is needed. The circuit is fully balanced such that the effect of bias-induced mismatches is eliminated. In addition, differential configuration is employed to minimize the fluctuation of the power and ground caused by the switching of the digital portion of mixed-mode circuits. A new differential negative current-current feedback mechanism is introduced to lower the input impedance and increase the bandwidth. The proposed amplifier is implemented in a 0.18 1.8V CMOS process and analyzed using SPICE. The results are presented.

TAM2L-209 -- Current Mirrors with Limiting of Linear Dynamic Range
Igor Filanovsky, *University of Alberta*

The paper describes two current mirrors with limiting of their linear dynamic range. The first circuit uses the difference between the absolute values of threshold voltages that exists in many CMOS technologies. The second circuit uses the threshold voltage variation caused by the body-effect. The calculation of their transfer characteristics is given as well as an example of application (second circuit) for stabilization of amplitude in the oscillator.

TAM2L-211 -- RF and Microwave Filters
Tuesday: 10:40 am – 12:00 pm
Chair: Jose Silva-Martinez
Texas A&M University

TAM2L-211 -- Automatic Tuning for Active-LC Filter
Hengsheng Liu and Aydin Karsilayan, *Texas A&M University*

An automatic frequency and Q tuning technique suitable for gigahertz active-LC bandpass filters is presented. An active-LC filter is designed to evaluate the tuning scheme. The circuit is designed using TSMC 0.35um process. A Simulation achieves a frequency tuning error of -0.2%, and Q tuning error of 2.1%.

TAM2L-211 -- Fully Integrated Bandpass Filters for Wireless Transceivers - Problems and Promises
William Kuhn, *Kansas State University*

Despite decades of research into developing true, single-chip radio transceivers, most commercial designs continue to rely on off-chip components for bandpass filtering functions. In a typical transceiver, narrow bandwidth filters are used for preselection, image-rejection, channel-selection, and power-amplifier harmonic attenuation. Implementing these filters on-chip remains nearly as challenging today as it was 10 years ago and few technologies have made it to commercial production. Exceptions to this include the sporadic adoption of Gm-C active filters into IF subsystems for channel-selection, and the occasional use of broad-bandwidth LC filtering in some front-end designs. In this paper, we review filter performance requirements and implementation alternatives, and overview the fundamental as well as technological constraints. Although commercial acceptance has been limited to-date, advances in the state-of-the-art continue to push on-chip filter technology forward, and the field holds much promise. Our goal is to highlight some recent achievements and to identify needed areas of research that may ultimately lead to more commercial application.

TAM2L-211 -- Design Considerations of Bandpass LC Filters for RF Applications
Ahmed Mohieldin, Edgar Sanchez-Sinencio, and Jose Silva-Martinez, *Texas A&M University*

This paper presents different design considerations of active Q enhanced LC bandpass filters. An architecture for implementing high order filters is proposed. It is using electric coupling to emulate the effect of the transformer thus providing bandwidth tuning with small passband ripple.

TAM2L-211 -- Optimized Synthesis of X Band Microstrip Side Coupled Bandpass Filters
Jon Putnam, George Branner, and Jessi Johnson, *University of California, Davis*

This paper discusses the synthesis of X band microwave bandpass filters. The techniques are unique in that filters are synthesized subject to geometrical constraints.

TAM2L-213 -- Nyquist Rate Data Conversion II
Tuesday: 10:40 am – 12:00 pm
Chair: Won Namgoong
University of Southern California

TAM2L-213 -- An On-chip GHz Undersampling Delta Modulator
Jing Huang and Jin Liu, *The University of Texas at Dallas*, and Mark Burns, *Texas Instruments Inc.*

An undersampling delta modulator capable of capturing GHz-range signals is designed and simulated successfully in 0.25um CMOS process. It converts high-frequency periodic waveforms into low-frequency

images, thus greatly facilitating signal rise and fall time measurement. When combined with on-chip signal processing, the undersampling delta modulator can be used to automatically adjust the rise and fall time of GHz-range signals.

TAM2L-213 -- Investigations Using Floating-Gate Circuits for Flash ADCs

Philomena Brady and Paul Hasler, *Georgia Institute of Technology*

Typically, high speed Analog to Digital converters are built using various forms of Flash converter architectures. However, all of these structures suffer from one major flaw, offsets. Whether these offsets are introduced from the resistive biasing network, mismatches in the comparators, or from other sources, extensive care must be taken to compensate for them. To compensate for these offsets, we investigated the use of floating-gate circuits in a 6-bit Flash ADC. By using the floating-gate circuits we are able to program the necessary reference voltages instead of depending on a resistive biasing network. The floating-gate circuits also enable us to compensate for any other offsets. In addition, programming the reference voltages reduces the power dissipation required for biasing the comparator array, and it allows us to implement nonlinear codes.

TAM2L-213 -- Fat Tree Encoder Design for Ultra-High Speed Flash A/D Converters

Daegyu Lee, Jincheol Yoo, Kyusun Choi, and Jahan Ghaznavi, *The Pennsylvania State University*

The thermometer code-to-binary code encoder becomes the bottleneck of the ultra-high speed flash ADCs. In this paper, the authors presented the fat tree thermometer code-to-binary code encoder that is highly suitable for the ultra-high speed flash ADCs. The simulation and the implementation results show that the fat tree encoder outperforms the commonly used ROM encoder in terms of speed and power for the 6 bit CMOS flash ADC case. Especially the speed improved almost double using the fat tree encoder, which in fact demonstrates the fat tree encoder as an effective solution for the bottleneck problem in the ultra-high speed ADCs.

TAM2L-214 -- IP, Embedded Cores, and Systems on a Chip II

Tuesday: 10:40 am – 12:00 pm

Chair: Wael Badawy

University of Calgary

TAM2L-214 -- A Parametric DCT Architecture for H.263+ Mobile Terminals Video Streaming

Guido Masera, Andrea Molino, Gianluca Piccinini, and Maurizio Zamboni, *Politecnico di Torino*

Due to recent wireless market explosion it is forecastable that in a near future, mobile terminals will deploy voice as well as true multimedia services. In this framework the need for low-power, multimedia oriented IP is felt. The main aim of this paper work is to discuss a parametric architecture for Discrete Cosine Transform. The proposed architecture is intended to be used as transform stage in a mobile H.263+ codec. What is striking about this core is that it sustain a full-motion PAL video streaming operating at a frequency of 74 MHz with 39 mW of dynamic power dissipation.

TAM2L-214 -- MAP decoder architecture: Soft IP for SOC

Mahmoud El-Assal, and Magdy Bayoumi, *University of Louisiana at Lafayette*

A soft IP for MAP decoder is presented. The Soft IP supports different design objectives, such as high performance and area efficient, which are passed as design parameters to the IP. FPGA platform will be used for developing the IP for rapidly prototyping the core. The IP is realized using VHDL and scripts that accept design specifications from the designer and automatically generate a synthesizable HDL for the required specifications developed. As of the day of submission, this work is still under development.

TAM2L-214 -- A Co-Processor for Real-Time Energy Estimation of System-On-a-Chip

Josef Haid, *Graz University of Technology*

Energy consumed by hardware running application software is often hard to estimate on large integrated circuits, such as System-On-a-Chip (SOC). As mobile electronic devices become increasingly important in our everyday life, advanced technologies are necessary to meet the constraints on low energy consumption and power aware system design. In this work a co-processor is presented, delivering the energy consumption to the application engineer in real-time. The co-processor is based on power macro-modeling, making any analogue measurement equipment obsolete to the application engineer after the SOC is characterized once.

TAM2L-214 -- SoC Interconnect in Deep Submicron

Mohamed Elgamel, Stacy Crochet, and Magdy Bayoumi, *University of Louisiana at Lafayette*

The migration to using Ultra Deep-submicron (UDSM) process, 0.25 mm or below has enabled the integration of complete electronic systems onto one single chip. These Systems-on-Chip (SoCs) introduce various challenges in terms of design flows and CAD tools. A design methodology that allows component reuse and intellectual property is necessary for achieving the required functionality, performance and testability while minimizing the cost and time to market. This design methodology relies on the use of a standardized connection interface like a shared bus, which presents increasing difficulties in (SoC). This paper describes research directions and various levels of design abstraction to increase the performance of interconnect. These directions include approaches to adopt new analytical models for interconnects and ways to face these challenges early in the design flow. To maximize the benefits of this paper, an extensive set of references is given.

TAM2L-216 -- VLSI Routing, Partitioning and Placement

Tuesday: 10:40 am – 12:00 pm

Chair: Robert Reese

Mississippi State University

TAM2L-216 -- Minimum Cost Complex Resource FPGA Partition with Performance Refining

Yu-Shan Hung, Chih-Hung Lee, Su-Fen Tseng, and Tsai-Ming Hsieh, *Chung Yuan Christian University*

In this paper, we provide a minimum cost partition with performance refining algorithm for complex resource FPGAs. The ILP solver, LINGO, is employed to find the number of the FPGA chips of each type to minimize the total resource cost. Then the delay analysis is performed on the given circuit such that we can find critical paths during circuit partitioning. Finally, a maximum matching based algorithm cooperated with node ordering based on delay information is used to partition the given circuit and map it into the corresponding resources of targeted FPGAs. Experiment results on the MCNC LGSynth91 benchmark show that our algorithm not only can implement test circuits with the minimum cost but also can further improve their performance.

TAM2L-216 -- Block Placement Using the Segment Tree Data Structure from Computational Geometry

Sarat C. Maruvada, Karthik Krishnamoorthy, and Florin Balasa, *University of Illinois at Chicago*

Since Murata et al. introduced the elegant topological representation of a block placement configuration called sequence-pair, there was a significant research effort in the field of encoding systems for non-slicing floorplans. This paper presents a block placement technique operating on the set of binary tree representations of the layout --called B-trees. The novelty of this approach is due to an efficient B*-tree evaluation based on a data structure called segment tree, mainly used in computational geometry. Experimental results using device-level analog placement problems as benchmarks confirm the efficiency of the novel exploration approach.*

TAM2L-216 -- A Genetic Algorithm for Mixed Macro and Standard Cell Placement

Theodore Manikas, *University of Tulsa,* and Marlin Mickle, *University of Pittsburgh*

The objective of mixed macro and standard cell placement is to arrange components on a chip such that the resultant layout area and interconnection wire lengths are minimal. A common approach is to divide the problem into separate macro cell and standard cell placement problems. However, this approach ignores the relationships between the macro and standard cells, which can affect the quality of the final solution. This paper describes a genetic algorithm that uses the relationship information to determine a more efficient placement solution.

TAM2L-216 -- A Module Placement Algorithm Based on Sequence Pair by introducing the concept of clustering

Su-Yuan Tseng, Chih-Hung Lee, and Tsai-Ming Hsieh, *Chung Yuan Christian University*

Chip area minimization and total wire length minimization are two main objectives of module placement / floor planning problem. Most of previous researches solve this problem by providing a simulated annealing based algorithm with a linear cost function composed by chip area and total wire length. However, due to consider the multiple optimization goals at the same time, it is very difficult to find the balanced point for deciding the weighted cofactors on each objective. In this paper, we firstly analyze the interconnection relation of nets among modules and further perform module clustering according to the analyzed result on interconnection. For each cluster, a pure area minimization oriented subfloorplan will be built by a sequence pair based simulated annealing algorithm. By concatenating the sub-sequences of subfloorplans, we can build the sequence-pair of an initial solution. Through the refinement on the initial solution, the final solution can be generated. Experimental results on MCNC benchmarks show that our approach is quite promising.

TAM2L-218 -- Networking Circuits and Systems

Tuesday: 10:40 am – 12:00 pm

Chair: Mingyan Liu

University of Michigan

TAM2L-218 -- Switch Fabric Design and Performance Evaluation: Metrics and Pitfalls

Gautam Kavipurapu, and Mehrdad Nourani, *The University of Texas at Dallas*

The rapid growth of the internet and the demand for carrying mixed mode traffic to deliver the commodity services, voice and data, at reasonable cost, to end users has put new pressures on the designers of switches and routers. The traditional architectures of routers with shared memory or crossbar are inefficient and fall short in their ability to meet this challenge. The need for faster optical switches fuelled by this rising demand is fraught with risks and fundamental physics problems that need to be addressed. We first examine the problem of designing a switch fabric that forms the core of the router as a multivariate optimization problem and in that context examine the limitations of the traditional crossbar or shared-memory approaches. We present a novel architecture that utilizes a combination of both space and time division multiplexing to deliver higher orders of throughput for a given switch size.

TAM2L-218 -- ATM Switch for 2.488 Gbit/s CATV Network on FPGA with a High-Throughput Buffering Architecture

Heikki Kariniemi, Jari Nurmi, *Tampere University of Technology*, Perttu Fagerlund, Janne Liitola, and Jani Alinikula, *Teleste Corporation*

This paper presents an ATM switch with a high-throughput buffering architecture and a new performance measurement system. The switch is designed for multiplexing and routing Digital Video Broadcasting (DVB) services over 2.488 Gbits/s Asynchronous Transfer Mode (ATM) Cable TV (CATV) backbone network. The buffering architecture is based on a crossbar switch with internal buffering but it also has features of shared

memory and output buffered switches. In addition to the buffering architecture the high throughput of this switch is based on an adaptive arbitration algorithm that is a used to schedule transfers of the cells from the cross-point buffers to the output buffers. This adaptive algorithm, which is a combination of Round Robin (RR) and Longest Queue First Served (LQFS) algorithms, provides starvation free service for the buffers with a small cell loss rate. Due to the internal buffering it was possible to use distributed arbitration that can easier achieve a high operation rate than one centralized arbiter. This paper also shows a quick and easy way of analyzing the performance of the presented ATM switch architecture. The high throughput of the switch is also verified using a new method of measuring the probability distribution of the filling of the buffers of the switch. Additionally this paper deals with a few implementation aspects, since the control logic and the internally buffered crossbar are implemented on a Field Programmable Gate Array (FPGA) circuit.

TAM2L-218 -- Analysis of Capacity Improvement in Adaptive OFDM Wireless Systems

Krishnaveni Ramasamy and Jong-Moon Chung, *Oklahoma State University*

With the exponential increase in number of mobile users, the quality of signal is reduced due to signal fading, roaming, and multipath effect in the RF channel. A unique solution is not possible since the channel characteristics vary at different times. This paper analyzes the spectral efficiency, optimization of power, bit error rate (BER) of the varying mobile Rayleigh fading channel by providing a comparison for Single Carrier, Multi Carrier, OFDM, AOFDM systems and suggests the efficient deployment of these systems according to the channel characteristics.

TAM2L-218 -- A Simple Synchronization Method Using Gold Code For M-ARY/DS Powerline Communications

Tadashi Suetsugu, and Marian Kazimierczuk, *Wright State University,* Katsutoshi Nakamura, *Fukuoka University*, and Mitsutomo Kawashima, *Ibiden Industries. Co.Ltd.*

A synchronization method to transmit a spreading code that consists of the PN sequence Mk and a Gold code of Mk+1 and Mk is proposed for the M-ary/DS power line communications. A demodulator can be simplified by this method. Simulation results are given for synchronization error rate and prediction error rate of the spreading code when transmitting the signal through a simple power line model.

TAM2L-219 -- Aerospace Applications of Modeling, Control, and Neural Netowrks

Tuesday: 10:40 am – 12:00 pm

Chair: Mark Motter

NASA Langley Research Center

TAM2L-219 -- Intelligent Flight Control: What are the Flight Research Programs and Why Develop this Technology?

James Urnes Sr, *The Boeing Company*

The Boeing Company is conducting a series of programs with NASA, the Navy, and the USAF that apply intelligent control technology to flight control systems. These control systems are designed to adapt to off-nominal damage or failure conditions. Reconfigurable control, artificial neural network models, self-learning neural networks, and matrix inverse control methods are some of the technologies used in these flight research projects. This paper will address the need for intelligent control and the general requirements for the design of intelligent systems. A description of the major intelligent controls programs Boeing is conducting will be given.

TAM2L-219 -- On Board Flight Computers for Flight Testing Small Uninhabited Aerial Vehicles

Charles Hall Jr, *North Carolina State University*

This paper will discuss two systems that were developed to support flight tests efforts. The Flight Computer System (FCS) was based on the DS2250 embedded controller. The FCS is small and lightweight, but it has limited I/O and computational capabilities which were overcome by using FCS networks. The analog to digital converter on the FCS was a novel design that would also produce a hybrid integration of the signal. The Linux In Flight Testing (LIFT) system was based on the use of COTS PC104 cards with a Real-Time Linux operating system. The RT Linux provides the hard real-time capability required for quality data collection and control system implementation. The LIFT system provides for expansion to satisfy complex mission requirements.

TAM2L-219 -- Adaptive Flight Control of Advanced Fighter Aircraft at High Angles of Attack

Anthony Calise, Matthew Johnson, and Yoonghyun Shin, *Georgia Institute of Technology*

In fighter aircraft at high angles of attack, unsteady aerodynamic effects such as wing rock and saturation of aerodynamic control effectors can lead to difficulty in control and maneuverability. This paper will demonstrate the use of a dynamic inverse based adaptive output feedback control method applied to an F-15 like aircraft model with thrust vectoring capability. The model includes a high-angle of attack (up to 60) aerodynamic model with unsteady effects added. The objective of the control design is to demonstrate adaptation to aerodynamic uncertainty in the form of both unmodeled parameter variations and unmodeled dynamics present in the nominal inverting design.

TAM2L-219 -- Identification of Aircraft Dynamics Using a SOM and Local Linear Models

Jeongho Cho, Jing Lan, Geetha Thampi, and Jose Principe, *University of Florida*, and Mark Motter, *NASA Langley Research Center*

Self-Organizing Map (SOM) is a powerful tool to produce topology preserving subspace mappings of high dimensional data. In this work we combine a SOM with a set of local linear models to identify potentially nonlinear nature of the plants and the large dimensionality of the spaces involved (many degrees of freedom and large dynamic range of parameters). Hence we compare different ways of producing the SOM (in the full space, in orthogonal subspaces and along each state variable), as well as fixed versus growing SOM topologies. The performance of the proposed algorithms is tested on simulated data obtained from a realistic aircraft model.

TAM2L-221 -- Detection and Enhancement

Tuesday: 10:40 am – 12:00 pm

Chair: Domenic Ho

University of Missouri

TAM2L-221 -- Limits on Echo Return Loss Enhancement on a Voice Coded Speech Signal

Mark Rages and K. C. Ho, *University of Missouri-Columbia*

Acoustic echo cancellation is a desirable feature for small cellular handsets that have significant acoustic coupling from speaker to microphone. Current echo cancellation techniques prefer an echo canceller to be placed at the wireless handset. Because echo cancellation requires much processing power it is beneficial to move the echo canceller to the base station, where power consumption will not be a constraint. This paper examines the feasibility of performing linear echo cancellation on a signal coming from a mobile at the base station. The mobile signal at the base station contains speech coding which may degrade the effectiveness of echo cancellation. The performance of linear echo cancellation on mobile echo encoded and decoded by a low

bit rate speech coders operating at 4 kbits/sec to 13 kBits/sec, including GSM full rate, G.723a, G.729, and AMR speech coders, was investigated. The best echo return loss enhancement achieved depends on the bit rate of the coder, and is usually less than 10 dB for the low bit rate operating range examined.

TAM2L-221 -- Wavelet Singularity Detection for Image Processing

Daniel Lun and Tai-Chiu Hsung, *The Hong Kong Polytechnic University*

The origin of the idea of wavelet singularity detection (WSD) can be traced back to the work of Jaffard. It was showed that the local regularity of an n-dimensional signal (which is measured through the Lipschitz exponent of the signal) can be estimated by analyzing its n+1-dimensional scale-space. Mallat further proposed that the Lipschitz exponent of a singularity can be estimated by tracing its wavelet transform modulus maxima (WTMM). Nevertheless, the tracing of WTMM is not just a tedious procedure computationally; ambiguity is often resulted in determining the relationship of a modulus maximum to a singularity. In that light, the wavelet transform modulus sum (WTMS) approach was proposed. In this paper, the applications of WTMM and WTMS in image denoising, compressed image deblocking, and scalable image coding are described. They show that WSD is a valuable tool for image processing and has widespread applications.

TAM2L-221 -- A Closed Form Frequency Estimator for a Noisy Sinusoid

H. C. So, *City University of Hong Kong*

Based on the linear prediction property of sinusoidal signals, a closed form unbiased frequency estimator for a real sinusoid in white noise is proposed. The frequency estimate derives from minimizing a constrained least squares cost function and it is simple to implement either in batch or recursive mode. The relationship of the proposed method with the well-known Pisarenko harmonic decomposer (PHD) is also examined. Computer simulations are included to contrast the estimator performance with the PHD as well as the Cramer-Rao lower bound.

TAM2L-221 -- Least Mean Square Algorithm for Unbiased Impulse Response Estimation

H. C. So, *City University of Hong Kong*

In this paper, a least mean square (LMS) type algorithm is devised for unbiased system identification in the presence of white input and output noise, assuming that the ratio of the noise powers is known. The proposed approach aims to minimize the mean square value of the equation-error function under a constant-norm constraint, and is equivalent to minimizing a modified mean square error function. Analysis of the algorithm shows that the estimates will converge to the true values in the mean sense. Computer simulations are included to corroborate the theoretical development and to evaluate the impulse response estimation performance of the LMS algorithm.

TAM2L-223 -- Image and Video Coding

Tuesday: 10:40 am – 12:00 pm

Chair: Edward Delp

Purdue University

TAM2L-223 -- Some Steps Towards a Unified Motion Estimation Procedure

Rudolf Mester, *University of Frankfurt, Germany*

After decades, motion estimation for video data still provides a variety of challenges, most notably in terms of robustness, precision and computational effort. In order to achieve further improvements w.r.t. established standard methods, it is useful to exploit explicit knowledge about the spatio-temporal statistics of the video signal and the noise, about the acquisition process, and the statistics of the motion itself. On the basis of realistic models for these entities, the relations between apparently different classes of motion estimation algorithms can

be uncovered further. We show how differential, tensor-based, matching-based, and correlation-based schemes can be cast into a common framework, which can be extended to comply with more complicated (and thus more realistic) motion situations.

TAM2L-223 -- An Efficient Region of Interest Coding for Image Compression

Men Long and Heng-Ming Tai, *University of Tulsa*

This paper presents a new method for region of interest (ROI) coding based on the embedded block coding with optimized truncation (EBCOT) paradigm. The proposed method reduces the priority of the less important region or background of an image, allowing the user to quickly view the ROI with higher quality without receiving the entire image bit-stream. Thus, it substantially saves the transmission time, storage space, and computational cost of image decompression. The unique characteristics of the new method lie in the combination of good ROI compression performance and low algorithm complexity. Experimental results indicate that the proposed method significantly outperforms the previous ROI coding schemes in overall ROI coding performance.

TAM2L-223 -- A New Method for JPEG2000 Region-of-Interest Image Coding: Most Significant Bitplanes Shift

Lijie Liu and Guoliang Fan, *Oklahoma State University*

Region-of-interest (ROI) image coding is one of the new features included in the JPEG2000 image coding standard, where two methods are defined, i.e., the Maxshift method and the generic scaling based method. In this paper, we will propose a new JPEG2000 compliant ROI coding method called Most Significant Bitplane Shift (MSBShift) that combines the advantages of the two standard methods. The MSBShift method not only supports arbitrarily shaped ROI coding without coding the shape, but also enables the flexible adjustment of compression quality in the ROI and background. Additionally, the new method can efficiently code multiple ROIs with different priorities in an image.

TAM2L-223 -- An Optimized Hybrid Vector Quantization for Efficient Source Encoding

Sunanda Mitra, Shuyu Yang, and Roopesh Kumar, *Texas Tech University*

Motivated by the efficiency of the well-known zero-tree scalar coding of wavelet transformed images, several attempts have been made recently to adopt similar methodologies in vector quantization (VQ). This latter approach, however, fails to retain fine details with a reasonable codebook size. We present a novel hybrid VQ scheme to preserve image details by creating a universal codebook of modest size with a combination of VQ and residual scalar coding of selective wavelet coefficients. Such codebooks, generated in an energy optimized wavelet domain, employ an efficient clustering technique and ensure minimal rate distortion even at very low bit rates.

TAM2L-225 -- Power Systems II

Tuesday: 10:40 am – 12:00 pm

Chair: Philip Yoon

University of Oklahoma

TAM2L-225 -- Data Quality and Grounding Considerations for a Medical Facility

Marcus Durham, *University of Tulsa*, and Robert Arnold *Oklahoma State University*

Medical facilities as well as most other commercial, industrial, and educational facilities depend heavily on telecommunications, data, and computer networks. These often experience problems with signal quality and noise because of the high-speed, low-level signals. In addition, there are serious issues that relate to electrical safety as well as computer grounding and communications. Topics such as the 11 different ground systems, connections to ground, avoiding potential difference, avoiding circulating currents, and wiring methods are

discussed. Three areas specific to networks require special attention. These are equipment bonding, isolated earth ground, and isolated power systems.

TAM2L-225 -- Advances in Gas Turbine Low Btu Combustion that Enable Integration of Power and Process Markets

Rex Tendick, *Syntroleum Corporation*

The Syntroleum Gas-to-Liquids (GTL) Process provides a unique Process/Power cogeneration opportunity for use in locations around the world. With this process, indigenous natural gas reserves can be monetized into ultra-clean diesel fuels for use in local fuel markets and for export, thus reducing importation of high sulfur diesel fuel that is harmful to the environment and earning project income and tax revenue for the host country. The clean fuels produced should earn a quality premium in markets such as the U.S., Europe, and Japan. Additionally, electrical power can be co-generated from the process in two ways. First, an air blown process produces a low Btu tail gas from its Fischer Tropsch reactors that can be used to fuel gas turbines to generate electricity. Second, steam generated from the exothermic Autothermal Reformers and Fischer Tropsch reactors can be used to drive steam turbines to produce additional electrical power. It should be noted that the low Btu tail gas, when combusted as a fuel in a gas turbine, produces significantly lower NOX emissions than natural gas and lowers maintenance costs, as well. The integrated approach of a GTL facility combined with an electrical power plant produces a steady stream of GTL clean diesel and a stable supply of electrical power. This paper will describe the advances in gas turbine technology in recent years that now allow the utilization of low Btu fuels in gas turbines for the power generation sector. In particular, the Low Btu combustion testing funded by Syntroleum and the equipment now available from two major gas turbine vendors will be discussed. Specific gas turbines well suited for integrating the GTL Process with the Power Sector will be reviewed.

TAM2L-225 -- Experimental Investigation of Distribution Transformer Aged Solid Insulation

Mirrasoul Mousavi and Karen Butler-Purry, *Texas A&M University*

In this paper, a laboratory test setup designed to perform insulation experiments is introduced. The electrode system utilized and the experimental procedure are described. The test results that highlight important aspects of insulation behavior concerning incipient fault detection and diagnosis is addressed. The results help identify particular phenomena that might happen when incipient fault initiates and develop a methodology to demonstrate them through an experimental setup.

TAM2L-225 -- Biomass A Renewable Source of Energy

Raj Sharma, *JNTU, Hyderabad*

Energy consumption in Asia is rising rapidly to keep pace with industrial development. The process of industrialization is set to continue, but should energy consumption simply rise with it? Thus, energy use can be rationalized with many benefits by using the renewable sources of energy. The nexus of some of the renewable sources of energy are: Bio-mass, Solar, Water, Wind. The main source of energy for the rural people who constitute the major part of the population of India, are biomass fuels. "Biomass" refers to organic matter such as wood, agricultural residues and crops that can be converted to energy. Biomass is of great eminence as it has plentiful resources. It provides economic, environmental, agricultural, and many other benefits. Several areas of applications are generation of electricity, heat, and steam and in combustible engines. India, being an agricultural country has sources of biomass in abundance and also has the capacity to provide a cost-effective and sustainable supply of energy, while at the same time aids to meet the greenhouse gas reduction targets. Biomass, possessing the potential of providing all the three forms of commonly used energies--electricity, heat and vehicle fuel is hence discussed in this paper.

TAM2P-140 -- VLSI Systems
Tuesday: 10:40 am – 12:00 pm
Chair: TBA

TAM2P-140 -- A Low-Power Reconfigurable Digital Pulse-Shaping Filter for an UTRA-TDD Mobile Terminal Receiver

Ronny Veljanovski, Jugdutt Singh, and Michael Faulkner, *Victoria University*

A novel reconfigurable digital pulse-shaping filter has been proposed for a mobile terminal receiver that can drastically reduce power dissipation dependant on adjacent channel interference. It automatically scales the number of filter coefficients by monitoring the in-band and out-of-band powers. This new filter performance was evaluated in a simulation UTRA-TDD environment because of the large near far problem caused by adjacent channel interference from adjacent mobiles and base stations. The UTRA-TDD downlink mode was examined statistically and results show that this reconfigurable filter can save an average of 75% power dissipation when compared to a fixed filter length of 41. This will prolong talk and standby time in a mobile terminal.

TAM2P-140 -- High Performance Low Power Video Compression Techniques

Wen-Tsong Shiue, and Weetit Wanalertlak, and Chee Lee, *Oregon State University*

Our paper presents a comprehensive solution for future digital video techniques with the constraints of the timing, memory storage and power dissipation such that the quality of video and/or image is still maintained. Our contributions in this paper include (i) software codec techniques such as fixed-point YUV components, factorized DCT, various DCT block sizes based on the quad tree data structure algorithm for the propose of reducing the complexity of the computations, increasing compression ratio, improving the performance, and (ii) hardware codec techniques such as dynamic voltage scaling incorporated in the hardware design stages for the chip design. Our benchmark results show that for an intra-frame with a 352x288 image size, 3157 frames can be processed in 22.23 seconds – almost 6x faster than the commercial MPEG2 [1] in the Linux GCC environment mounted at the Pentium III 866MHz laptops. Furthermore, the power consumption is reduced by 23% due to the techniques of dynamic voltage scaling incorporated in the hardware design.

TAM2P-140 -- Implementation of Wavelet Transform for Video Compression Applications

Mahesh Khekhenchery, Paul Salama, and Maher Rizkalla, *Indiana University - Purdue University Indianapolis*

Transform based image compression schemes involve the transformation of spatial information into another domain. The goal of the transformation is a compact, complete representation of the image. In this paper we describe the implementation of the Wavelet Transform using the Filter banks approach and the lifting scheme.

TAM2P-140 -- Implementation of 3D-DCT Based Video Encoder/Decoder System

Mohamed Abdel Halim and Aly Salama, *Cairo University*

3D-DCT technique is used in Video system to eliminate the need for motion vectors computations in the encoder or motion compensation computations in the decoder. This paper focuses on the Hardware implementation of the Video Encoder/Decoder system design. A complete design of the quantizer and VLC in the encoder side as well as design of dequantizer and VLD in the decoder side are implemented to complete the system. The system is designed using VHDL language and is targeted on one of the well-known Field Programmable Gate Arrays (FPGAs) provided by ALTERA Corp. and simulated using different sample inputs.

TAM2P-140 -- Floating Point Fast DCT Implementation

Maher Rizkalla, Paul Salama, Mohamed El-Sharkawy, and Bulent Dukel, *Indiana University/Purdue University,*

A 32-bit floating point; one-dimensional discrete cosine transform unit was designed based on the Vetterli and Ligtenberg fast DCT flow-graph using Mentor Graphics tools. The floating-point algorithm and the VHLD code of the DCT unit is described, and the simulation results of the output are presented

TAM2P-140 -- Implementation of a Programmable Phased Logic Cell

Mahir Aydin and Cherrice Traver, *Union College*

A phased logic FPGA does not require a global clock; it accomplishes its synchronization by encoding value and timing information of a single bit in two separate wires. In this project, two separate standard cell designs for a phased logic FPGA were simulated, fabricated in 0.5-micron and 1.5-micron CMOS technologies, and tested successfully.

TAM2P-140 -- On the Use of Wavelet Transforms in Testing for the DNL of ADCs

Rion Marshall and Cajetan Akujuobi, *Prairie View A & M University*

This paper evaluates the use of wavelet transforms in testing for the differential non-linearity (DNL) of ADCs. A MATLAB algorithm is developed to implement the Haar Wavelet Transform to perform the test. A comparison is then made between the wavelet and the histogram-based tests.

TAM2P-140 -- A High-Throughput Pipelined Architecture for Blind Adaptive Equalizer with Minimum Latency

Masashi Mizuno, Kenji Ueda, James Okello, and Hiroshi Ochi, *Kyushu Institute of Technology*

In this paper, we propose a pipelining architecture for the FIR portion of the Multilevel Modified Constant Modulus Algorithm (MMCMA). We also provide the correction factor that mathematically converts the proposed pipelined adaptive equalizer into an equivalent non-pipelined conventional MMCMA based equalizer. The proposed pipeline method uses modules with 6 filter coefficients, resulting in an overall latency of a single sampling period, along the main transmission line. The basic concepts of the proposed architecture, is to implement the FIR filter and the algorithm portion of the equalizer, such that the critical path has one complex multiplier and two adders.

TAM2P-140 -- ASIC Implementation of the Discrete Wavelet Transform

Michael Eckbauer, *GE,* Paul Salama, Maher Rizkalla and Mohamed El-Sharkawy, *Indiana University - Purdue University Indianapolis,*

Wavelets are an important and powerful signal processing tool. We describe the VHDL implementation of the constituent parts of the decomposition and reconstruction units and the top down design process used for custom IC design. The design was simulated, synthesized and optimized using CAD design tools from Mentor Graphics Corporation.

TAM2P-140 -- Area Efficient GF(p) Architectures for GF(p^m) Multipliers

Jorge Guajardo, Thomas Wollinger, and Christof Paar, *Ruhr-Universitaet Bochum*

This contribution describes new GF(p) multipliers, for p > 2, specially suited for GF(p^m) multiplication. We construct truth tables whose inputs are the bits of the multiplicand and multiplier and whose output are the bits that represent the modular product. However, contrary to previous approaches, we don't represent the elements of GF(p) in the normal binary positional system. Rather, we choose a representation which minimizes the resulting Boolean function. We obtain improvements of upto 35% in area when compared to previous approaches for small odd prime fields. We report transistor counts for all multipliers with p

TAM2P-140 -- A BIST Scheme for Testing the Interconnects of FPGAs

Mohammed Niamat and Mohammed Jamali, *U of Toledo*, Rajesh Nambiar, *Intel*

This paper discusses a new testing scheme for testing the interconnect resources in the Xilinx XC4000 series Field Programmable Gate Arrays (FPGAs). The scheme is based on the concept of Built In Self Test (BIST), which subdivides the test problem into a Test Pattern Generator (TPG), a Circuit Under Test (CUT) and an Output Response Analyzer (ORA). The research involves the location and detection of single-stuck-at and bridging and open faults that might be present in the interconnect network. The test responses obtained at the output of the ORA are stored in the Look Up Table (LUT) of the Configurable Logic Block (CLB) so that the faulty interconnect can be detected and located. This testing scheme ensures high reliability, increased fault tolerance capacity and provides maximal fault coverage. Reduced system time, zero circuit overhead and unity test resolution are some of the highlights of this new testing scheme.

TAM2P-140 -- A BIST Scheme for Testing a Multiple FPGA System

Mohammed Niamat and Ramachandra Jogu, *University of Toledo*

In this paper, an efficient Built-In Self Test (BIST) scheme for testing a multiple Field Programmable Gate Array (FPGA) system is presented. A multiple FPGA system is defined as a group of FPGAs on the same board or system. The proposed scheme can not only detect faults within the configurable logic blocks (CLBs) of the FPGAs being tested, but can also locate and identify the component within the CLB that is faulty.

TPM1L-209 -- Sensor Electronics

Tuesday: 2:00 pm– 3:20 pm

Chair: Franco Maloberti

University of Texas at Dallas

TPM1L-209 -- Data Converters for Sensor Systems

Piero Malcovati, *Pavia University,* Franco Maloberti, *UTD*

Sensors are becoming relevant elements for integrated systems. In the near future silicon sensors and digital signal processors will permit a powerful processing of the information related to physical and chemical quantities. Also the digital section will permit the designer to correct, calibrate and compensate the limitations of silicon sensors. All the above will be made possible by the interfacing action of data converters. Base on signal level, bandwidth and required resolution the designer must select the proper data converter architecture. This paper presents system and design strategies and trade-off for integrated sensor systems.

TPM1L-209 -- A New Wide Dynamic Range Fixed point ADC for FPAs

Jehyuk Rhee and Youngjoong Joo, *Arizona State University*

CMOS image sensor system has several clear advantages over CCD image sensor system: selective readout, low power, small size, high frame rate, on-chip functionality, and low cost [1]. However CCD image system still dominates over digital camera market, because the CMOS image system has a poor dynamic range (DR) and peak signal-to-noise ratio (SNR). In this paper, we propose a new enhanced DR and peak SNR CMOS image sensor with pixel level analog-to-digital converter (ADC). The proposed reset technique increases the well capacity of the imager. Consequently, DR and peak SNR are increased simultaneously while other DR enhancement schemes increase only DR. We designed and simulated the proposed circuit and achieved 12bit resolution with 1000fames/sec. Power consumption per each pixel is 50nW. DR is enhanced by 36dB and peak SNR is enhanced by 18dB.

TPM1L-209 -- A Universal Micro-Sensor Interface Chip with Network Communication Bus and Highly-Programmable Sensor Readout

Jichun Zhang, Kun Zhang, Zhigang Wang, and Andrew Mason, *Michigan State University*

This paper presents a Universal Micro-Sensor Interface(UMSI) circuit designed for low power Microsystems, which support multiple sensors and actuators. This all-inclusive chip contains the necessary reference, readout, control, and communication circuitry to connect a range os capacitive, resistive, voltage, and digital output devices to system control hardware. Fabricated in a foundry 3M 2P 0.5um CMOS process, the die occupies 2.22mm x 2.22mm and draws 6.7uA to 4mA,(depending on configuration) from a 3V supply. The chip is packaged in LCC52. Preliminary test results show the chip to be completely functional and within design specifications.

TPM1L-209 -- A Mixed-Signal IC for Multiple Cortical Stimulation Strategies

Jonathan Coulombe, Louis-Xavier Buffoni, and Mohamad Sawan, *Ecole Polytechnique de Montreal*

We present an integrated mixed-signal circuit dedicated for electrical stimulation. The chip has 4 channels using 4-electrode os each, to be connected directly on a square 16-electrode matrix. The circuit is designed for maximum flexibility and safety. It allows stimulation to be monopolar as well as bipolar, and uses a configurable communication protocol, reducing the transfer rate requirements according to the stimulation strategy used. Low power is achieved using dual-voltage supply. Finally, to ensure safe stimulation, characterization and troubleshooting after implantation of the chip, voltage monitoring of any of the 16 electrodes is possible using a rail-to-rail amplifier that can be shut-down for lowest power consumption. The circuit has been fabricated and tested in a CMOS 0.18 micron process.

TPM1L-211 -- RF and Microwave Amplifiers and Mixers I

Tuesday: 2:00 pm– 3:20 pm

Chair: Danny Pinckley

Motorola

TPM1L-211 -- On the Feasibility of Cascaded Single-Stage Distributed Amplifier Topology in Digital CMOS Technology

Apisak Worapishet, Mitchai Chongcheawchamnan, and Sarayut Srisathit, *Mahanakorn University of Technology*

Feasibility of the cascaded single-stage distributed amplifier (CSDA) structure over the classical distributed amplifier for ultra broadband amplification in CMOS technology is investigated in this paper. A number of unique benefits gained from the CMOS CSDA are highlighted along with some important analysis and helpful design hints. Designed and simulated in standard digital 3.3V 0.35um CMOS process with realistic parasitic models, a prototype design of a 4-stage CMOS CSDA provides 21dB power gain at 5GHz bandwidth, more than -10dB input/output return loss, larger than -7.3dBm 3rd-order input intercept point (IIP3) and dissipates less than 132mW from a 2.2V power supply.

TPM1L-211 -- Dual-Band Switchable Low Noise Amplifier for 5-GHz Wireless LAN Radio Receivers

Wen-Shen Wuen and Kuei-Ann Wen, *National Chiao Tung University*

The paper presents a dual-band switchable low noise amplifier implemented in 0.25-um CMOS technology for 5-GHz wireless local area network (WLAN) applications. Equipped with a PMOS capacitor together with the inductive load, the LNA is able to operate at the lower or the upper band at 5-GHz by 1-bit control signal. The LNA exhibits over 17 dB power gain, 3.5 dB noise figure and input 1-dB compression point -23 dBm in both frequency bands. The LNA draws 9.5 mA from 2.5 V supply.

TPM1L-211 -- A New RF CMOS Mixer with a High Performance in 0.18u Technology

Rami Salem and Mohammed Tawfik, *Mentor Graphics,* Hani Ragaie, *Ain Shams University*

In this paper, a new high linear radio-frequency CMOS mixer is presented. The new mixer is derived from the basic Gilbert multiplier. It achieves an outstanding linearity since the new topology does not contain any tail current branches. A CMOS transistor pair is instead applied to the four cross coupled commutating transistors. Simulations of the extracted layout results show a high linearity improvement over the basic Gilbert mixer, with IIP3 of 31 dBm in 0.8u and 20dBm in 0.18u. Simulations also shows 6dB improvement in the mixer's conversion gain in 0.18u over 0.8u, with 3.2mW power consumption. The new mixer's test chip layout and its extracted simulation characteristics in both technologies are presented.

TPM1L-211 -- A Novel CMOS Front-end Circuit with Low Power,Low Noise and Variable Gain for 5-GHz WLAN Applications

Min Lin, Haiyong Wang, Yongming Li, and Hongyi Chen, *IME of Tsinghua University*

Incorporating the low-IF architecture, a 5-GHz WLAN receiver front-end chip is implemented in a 0.18¦Ìm CMOS technology. The chip contains a single-in differential-out low noise amplifier with 1.5dB noise figure (NF), 25dB voltage gain and less than 13mW power consumption, a folded structure downconversion mixer with 9.9dB single side band noise figure (SSB NF), 13.7dB voltage gain and +2.7dBm IIP3, consuming 10mA current under a 2V supply voltage. The chip also has a 12dB gain adjustment through a VGA cell placed in parallel with LNA¡¯s input.

TPM1L-213 -- Testing and BIST I

Tuesday: 2:00 pm– 3:20 pm

Chair: Degang Chen

Iowa State University

TPM1L-213 -- A Novel Approach to Iddq Testing of Mixed-signal Integrated Circuits

Ashok Srivastava and Srinivas Aluri, *Louisiana State University*

This paper presents an effective built-in current sensor (BICS), which has a very small impact on the performance of the circuit under test (CUT). The proposed BICS works in two-modes the normal mode and the test mode. In the normal mode the BICS is isolated from the CUT due to which there is no performance degradation of the CUT. In the testing mode, our BICS detects the abnormal current caused by permanent manufacturing defects. Further more our BICS can also distinguish the type of defect induced (Gate-source short, source-drain short and drain-gate short). Our BICS requires neither an external voltage source nor current source. Hence the BICS requires less area and is more efficient than the conventional current sensors. The circuit under test is a 10-bit digital to analog converter using charge-scaling architecture.

TPM1L-213 -- A Histogram Based AM-BIST Algorithm for ADC Characterization Using Imprecise Stimulus

Kumar Parthasarathy and Le Jin, *Iowa State University*, Turker Kuyel, *Texas Instruments Inc, Dallas*, Degang Chen and Randall Geiger, *Iowa State University*

A new Built-In-Self-Test (BIST) strategy for characterizing Analog-to-Digital Converters (ADCs) has been proposed. In contrast to most existing BIST approaches which require precise stimuli that are challenging to generate on-chip, the proposed method incorporates a digital signal processing algorithm that is tolerant to very imprecise and easily generated stimuli. Preliminary simulation results show that with a 5-bit linear input signal, the trip points of a 11-bit Flash ADC can be identified to better than 0.5LSB and by incorporating a built-in calibration circuit, the trip point error can be decreased from an uncalibrated 15 LSB level (7-bit performance) to less than 0.5 LSB (11-bit performance) or better.

TPM1L-213 -- A Blind Identification Algorithm for Digital Calibration of Pipelined ADC

Le Jin, Kumar Parthasarathy, *Iowa State University*, Turker Kuyel, *Texas Instruments Inc, Dallas*, Degang Chen and Randall Geiger, *Iowa State University*

A blind identification based algorithm for calibration of pipelined ADC is discussed in this paper. In contrast to traditional approaches that use one highly precise input stimulus to characterize the device, the approach adopted here is based on providing multiple inputs with nonlinearities of separated spectrum to the device-under-test (DUT). A correction code for each output of ADC is determined, which is then used to calibrate the device. Simulation results show that using the algorithm, trip point error of a 16-bit pipelined ADC with original INL of hundreds of LSBs can be decreased to less than 1 LSB, while input signals of 6-bit linearity are identified to more than 12-bit accuracy. The relaxed requirement of the input signal makes it practical to be generated on-chip and hence is a promising solution for Analog and Mixed-signal Built-In-Self-Test (AMBIST).

TPM1L-213 -- On-Chip iDD Pulse Response Method Using a High-Speed Dynamic Current Sensor

Gladys Ducoudray and Jaime Ramírez-Angulo, *New Mexico State University*

This paper presents a built-in self-test on-chip testing scheme for analog, digital and mixed-signal circuitry compatible with the IEEE 1149.4 mixed-signal test bus standard. A high-speed dynamic current sensor is described. Simulation results are provided for the high-speed dynamic current sensor being used to measure the supply current of analog and digital devices. Simulation results include iDD waveform of defect-free circuits, for circuits with parametric/global faults, and circuits with catastrophic faults. This testing technique serves as an

early screening method for defect-free circuits and will potentially allow a fault-free IC to enter the market in significantly less time.

TPM1L-214 -- Low Power Circuits and Architectures I

Tuesday: 2:00 pm– 3:20 pm
Chair: Lex A. Akers
University of Missouri

TPM1L-214 -- Adiabatic Circuits for Low Power Logic

Lex Akers and Ragina Suram, *University of Missouri*

Adiabatic logic circuits offer significant reductions in power dissipation when compared with standard static CMOS design. However, many implementation issues remain to be solved. This paper will discuss low power design and then focus on adiabatic logic circuits and the required power clock needed to drive them. A new power clock is presented which does not utilize any external components and provides the gradual rise, hold, and fall times required for adiabatic logic.

TPM1L-214 -- Ultra Low Power 1-Bit Adder Cells

Tarek Darwish and Magdy Bayoumi, *University of Louisiana at Lafayette*

Supply voltage scaling is considered to be an effective technique for reducing power consumption of digital CMOS circuits. But such approach has a detrimental effect on system performance, which renders it impractical for many applications. In some applications, where power consumption is of critical importance, supply voltage scaling can be reasonably effective. In this paper, a set of adders is presented, and the supply voltage scaling technique is applied and the different adders are analyzed at a range of supply voltage levels (1.8 - 0.15 Volts). It is found that at very low supply voltage levels, the performance experiences immense deterioration. Moreover, for a fixed frequency of operation, the lowest supply voltage level attainable depends on circuit structure.

TPM1L-214 -- Energy-aware Multiplier Design in Multi-rail Encoding Logic

Jia Di and JiannShun Yuan, *University of Central Florida,* and Michael Hagedorn, *Theseus Logic Inc.*

Energy-awareness indicates the scalability of the system energy with changing conditions and quality requirements. A novel technique, Signal Bypassing and Zero Insertion, to design energy-aware multiplier in multi-rail encoding logic is developed. The results show that multi-rail energy-aware designs have advantages not only in energy saving, but also in delay reduction.

TPM1L-214 -- A Low-Power 2.1 GHz 32-bit Carry Lookahead Adder Using Dual Path All-N-Logic

Ge Yang, *University of CA, Santa Cruz*

A high-speed, low-power 32-bit carry lookahead adder is presented. We have developed Dual Path All-N-Logic(DPANL) and applied to 32-bit adder design for higher performance. The speed enhancement is mainly due to reduced capacitance at each evaluation node of dynamic circuits. This adder can operate at frequencies up to 2.1GHz for 0.35um 1P4M CMOS technology and is 31.3% and 27.3%faster than the adders using All-N-Transistor(ANT) and All-N-Logic(ANL), respectively. It also consumes 29.2% and 15.4% less power than the ANT adder and ANL adder, respectively.

TPM1L-216 -- VLSI Synthisis I

Tuesday: 2:00 pm– 3:20 pm

Chair: Mitch Thornton

Mississippi State University

TPM1L-216 -- Control versus Compute Power within a LEDR-style Self-timed Multiplier with Bypass Path

Robert Reese and Sakkina Sikandar-Gani, *Mississippi State University*

The design of a self-timed multiplier using level-encoded dual rail IO is presented. This multiplier is meant to be used as an element within a Phased Logic computing system. Phased Logic is a design methodology that allows automated translation from a clocked netlist to a self-timed netlist. A principle concern with Phased Logic compute blocks is the ratio of the power consumed by the control logic used for dual rail IO signal decoding/encoding and arrival detection versus the power needed for the actual computation. Post-layout simulation results from an 8x8=16 implementation which uses a CSA array mapped to a 0.5u standard cell library is used to extrapolate the control/compute power ratio for different sized multipliers of the same architecture. The multiplier control logic also incorporates a bypass path allowing early output generation if the multiplier result is not needed during this compute cycle. Simulation results from a mixed-operation datapath demonstate how this can significantly increase the throughput in a Phased Logic system.

TPM1L-216 -- Utilizing BDDs for Disjoint SOP Minimization

Goerschwin Fey and Rolf Drechsler, *University of Bremen*

The application of Binary Decision Diagrams (BDDs) as an efficient approach for the minimization of Disjoint Sums-of-Products (DSOPs) is discussed. DSOPs are a starting point for several applications. The use of BDDs has the advantage of an implicit representation of terms. Due to this scheme the algorithm is faster than techniques working on explicit representations and the application to large circuits that could not be handled so far becomes possible. Theoretical studies on the influence of the BDDs to the search space are carried out. In experiments the proposed technique is compared to others. The results with respect to the size of the resulting DSOP are as good or better as those of the other techniques.

TPM1L-216 -- Information Measures in Detecting and Recognizing Symmetries

Denis Popel, *Baker University*

This paper presents a method to detect and recognize symmetries in Boolean functions. The idea is to use information theoretic measures of Boolean functions to detect sub-space of possible symmetric variables. Coupled with the new techniques of efficient estimations of information measures on Binary Decision Diagrams (BDDs) we obtain promised results in symmetries detection for large-scale functions.

TPM1L-216 -- Technology-Independent Delay Optimization of Complex CMOS Circuitries

Peter-Michael Seidel, *Southern Methodist University*

It is often difficult to distinguish between the qualities of the technological realization of a complex circuit and the contribution of the underlying algorithm for the logic implementation. To extract these two qualities from each other, technology-independent analysis of circuitries becomes important. Technology-independent hardware models have often been accused of lacking level of detail in analyzing and treating design choices of the implementation. More detailed hardware models on the other hand often depend on the technology and process that is used for implementation. Recently, Sutherland et al. have introduced the hardware model of "logical effort" which allows a rigorous, but technology-independent treatment of gate delays, fanouts, optimized gate sizing and buffer insertion. This model has been introduced and used for small circuitries and simple paths. Our extension is the application of this model for technology-independent delay optimization of complex circuitries. We are applying this model to the complex circuitry of a fast FP-adder implementation. We explain

steps and procedure that are required to compute optimal gate sizes and optimal buffer insertion for this implementation. Finally we discuss the potential of our delay optimization procedure to be automated for arbitrary circuits.

TPM1L-218 -- Advanced Networking Systems I

Tuesday: 2:00 pm– 3:20 pm

Chair: Bon-Jin Ku

Oklahoma State University

TPM1L-218 -- Burst Erasure Correction to Improve the Efficiency of Broadband CSMA/CD

John Metzner, *Pennsylvania State University*

Assume a broadcast network with a central station. All senders send to the central station, and the central station rebroadcasts all receptions on a different band. In standard CSMA/CD, all senders stop when a collision is detected. In the suggested modified algorithm, exactly one continues to send. A colliding sender can know if it was the first to arrive at the central station. If so, it continues to send, else it stops. The one that continues to send incurs an observable-length erasure burst, and appends a redundant part to its frame to allow filling in the burst erasure

TPM1L-218 -- Dual Stage Hybrid Restoration Protocol for Optical Networks

Jong-Moon Chung and Vizayakumar Kotikalapudi, *Oklahoma State University*

The advent of broadband communication technologies that enabled ultra-speed data transfer increased the demands of people. There is a marked shift towards video, multi-media and other throughput intensive applications. To support these next generation communication needs, not just a high-speed transfer but also high reliable networks as needed. As increasing number of real time applications become involved, the major concern for these highly dependable networks is to have uninterrupted service. To ensure this uninterrupted service, the restoration time in case of fiber cut or node failure has to be extremely low as disruption in high-speed networks causes considerable loss even in an extremely small duration. The restoration strategies like line restoration and path restoration, which are designed to restore yesterday's networks, are not capable enough to support real time applications in high-speed environments of tomorrow. To address this problem, we propose a dual-stage hybrid restoration protocol (DHRP) for achieving survivability in optical networks. The spare capacity calculation is done implementing the proposed protocol and the results are analyzed.

TPM1L-218 -- Impact of Self-Similarity on Performance Evaluation in Differential Service Networks

Zhi Quan and Jong-Moon Chung, *Oklahoma State University*

Priority queueing has currently become a popular research topic as a low-cost method to bring quality of service (QoS) to differential services (DS) networks. However, there are so many uncertain issues before deploying it to the real Interne, which are concerned with quantitative network performance. On the other hand, the impact of self-similarity on network performance has received more and more attention recently, which makes the study of DS network much more challenging. The purpose of this paper is to study QoS measures in priority queues under self-similar traffic. We first introduce the techniques that we used to generate self-similar network traffic, as well as the methods how to design and implement priority queues by using OPNET. Then we present our statistical results from a simulation study with synthesized self-similar traffic. Our study results show that self-similar traffic, compared with traditional short-range dependent (SRD) models, requires longer queues and, thus larger buffers in the DS network design.

TPM1L-218 -- Simulation of FNBDT over Internet and 3G Wireless Networks

Edward Daniel and Keith Teague, *Oklahoma State University*

The Future NarrowBand Digital Terminal (FNBDT) is a signaling plan, initiated by the government, that describes a new approach to providing interoperable secure multimedia communications between compatible devices over like and unlike networks. Non-ideal network behavior affects the usability and operation of FNBDT. Mathematical simulations for several configurations of wired and wireless networks and different network performance characteristics are presented. Results illustrate tradeoffs of network conditions and the performance of FNBDT.

TPM1L-219 -- Adaptive Systems I

Tuesday: 2:00 pm– 3:20 pm

Chair: Edward Wilson

Intellization

TPM1L-219 -- On-line, Gyro-based, Mass-property Identification for Thruster-controlled Spacecraft

Edward Wilson and Chris Lages, *Intellization*, and Robert Mah, *NASA Ames Research Center*

Spacecraft control, estimation, and fault-detection-and-identification systems are often affected by unknown variations in the vehicle mass properties. It is often difficult to accurately measure inertia terms on the ground, and mass properties can change on-orbit as fuel is expended, the configuration changes, or payloads are added or removed. Algorithms that identify the center of mass location and the inverse of the inertia matrix using gyro signals are presented. They are applied in simulation to the X-38 and Mini-AERCam vehicles under development at NASA-JSC, and in hardware on an air-bearing spacecraft simulator at the NASA-Ames Smart Systems Lab.

TPM1L-219 -- A Radial Basis Function Implementation of the Adaptive Dynamic Programming Algorithm

George Lendaris, *Portland State University*, Chadwick Cox and Richard Saeks, *Accurate Automation Corp.*, and John Murray, *State University of New York at Stony Brook*

Adaptive Dynamic Programming constitutes a potentially powerful approach to optimal control theory where one iteratively updates an approximation to the Bellman cost functional. The technique is applicable to a broad class of nonlinear networks with unknown dynamics and is guaranteed to: converge to the optimal control with stepwise stability. The goal of this paper is to describe an implementation of the Adaptive Dynamic Programming algorithm in which a radial basis function is used to define the approximate cost functional, which is updated locally in the neighborhood of the state trajectory each time the system is run. An application of the algorithm to a nonlinear flight control problem with unknown aircraft dynamics is presented.

TPM1L-219 -- A Reconfigurable Architecture Suitable For Adaptive Multi-Resolution Processing

Mohamed Helaoui, Lirida Naviner, and Jean François Naviner, *Ecole Nationale Superieure des Telecommunications (Paris)*, Marcelo De Barros, *Universidade Federal da Paraiba (Brazil)*, and Adel Ghazel, *Ecole Superieure des Communications de Tunis*

This work deals with adaptive multi-resolution processing. We present an adaptive filter bank structure for sub-band splitting of signals in order to match the system requirements. Reconfiguration of the filter bank is carried out according to an evolutionary algorithm. The architecture is designed to allow a dynamic reconfiguration of the number and the width of each sub-band

TPM1L-219 -- Unsupervised Self-Organizing Adaptive Fuzzy Controller (SOAFC)

Asaad Makki, *Ford Motor Company*, Hafiz Khafagy, *EESE*, and Ka. Cheok, *Oakland University*

Supervised adaptive fuzzy controllers have good learning capability [7]. The main problem is how to obtain an on-line input/output data pattern capable of maintaining the required characteristics of the over all system. A proposed solution is the design of on-line unsupervised controller that has self-tuning and self-constructing features. In this paper, the development of unsupervised Self-Organizing Adaptive Fuzzy Controller (USOAFC) will be introduced. USOAFC is a novel idea for designing a controller that is suitable for on-line applications. It starts with some preliminary rules and it sets out to construct the necessary rules required to drive the system to achieve the required performance. It also has the ability to tune the existing rule. The algorithm is contracting and tuning the existing rules on-line. It is able to handle the human knowledge. It is able to deal with the ambiguity, uncertainty and un-stability of the system. The algorithm is simple to understand and easy to apply to many processes.

TPM1L-221 -- Mixed Signal and Signal Conversion Processing I

Tuesday: 2:00 pm– 3:20 pm

Chair: J. W. Bruce

Mississippi State University

TPM1L-221 -- A 5mhz Silicon CMOS Hierarchical Boost DC-DC Converter Design Using Macromodels for a 1u Process

Mark Hooper, *Georgia Institute of Technology*, Jeff Hall, *ON Semiconductor*, and Steve Kenney, *Georgia Institute of Technology*

This work presents an innovative design of a high frequency and potentially highly efficient boost DC-DC converter with an input voltage of 2.7-3.3 Volts and with a programmable output voltage of 4-9 Volts. Current sourcing capability is between 40mA-360mA. A low power boost DC-DC converter designed in CMOS which partially uses circuit macromodels --designed and tested using Cadence tools-- for an all CMOS silicon process illustrates this design. The key features of this design are very high switching frequency, reconfigurability, silicon all CMOS implementation, and mixed signal simulation capability.

TPM1L-221 -- Design of COR Sigma-Delta A/D Converters Amenable to Capacitor Scaling in Switched-Capacitor Hardware Implementations

Neil A. Fraser, *Edgewater Computer Systems*, and Behrouz Nowrouzian, *University of Alberta*

It is well known that the cascade-of-resonators (COR) Sigma-Delta A/D converters achieve high signal-to-quantization-noise ratio (SQNR) levels in virtue of the fact that the constituent noise transfer function zeros are located at real frequencies. The existing techniques for the design of COR Sigma-Delta A/D converters fail to take into account the capacitance spread and the total capacitance in a corresponding switched-capacitor hardware implementation. This letter presents a novel approach to the design of COR Sigma-Delta A/D converters yielding small capacitance spread as well as small total capacitance. This is achieved by making the constituent feedforward capacitors mirror images of the corresponding feedback capacitors. These conditions are themselves satisfied by ensuring that the signal transfer function is made complementary to the noise transfer function. The application of the proposed approach to the design of a hitherto COR A/D converter results in a 450% reduction in the capacitance spread, a 340% reduction in the total capacitance, while yielding the same achievable SQNR and dynamic range.

TPM1L-221 -- An Overview of Circuits & Devices Research on SOI Technology for Analog/Mixed-Signal Systems

Benjamin Blalock and Stephen Terry, *The University of Tennessee,* Brian Dufrene, *Mississippi State University*, Chandra Durisety, and Lee Kee Yong, *The University of Tennessee*, Sorin Cristoloveanu, *ENSERG, Grenoble, France,* and Mohammad Mojarradi, *Jet Propulsion Laboratory*

SOI technology has become the commercial technology of choice for both high performance and low power digital applications. By comparison, analog development in SOI is still in its infancy. To help emphasize analog/mixed-signal opportunities in SOI, both for circuits and new devices, this paper provides a sampling of SOI research at the University of Tennessee. Circuit highlights include an operational amplifier with automatic offset cancellation, a VCO-based ADC, and body-driven analog circuits. The G4-FET, a four-gate transistor in SOI, will be introduced. Floating-gate devices on SOI will also be presented, including their application to post-process trimmable analog circuits

TPM1L-221 -- CMOS Current Mode Interpolating Flash Analog to Digital Converter

J.A. Bell and J.W. Bruce, *Mississippi State University*

A high speed CMOS current-mode interpolating flash analog-to-digital converter capable is proposed. The design uses generic cells to generate all current comparator inputs. The proposed interpolation technique reduces the transistor count and power consumption of a pure flash implementation while improving SNR, SFDR, and DNL. Five-bit interpolating flash and pure flash designs were implemented in 0.5 mm CMOS to compare performance characteristics.

TPM1L-223 -- Signal and Image Analysis I

Tuesday: 2:00 pm– 3:20 pm

Chair: Joe Havlicek

University of Oklahoma

TPM1L-223 -- Deep Space 1 Mission and Observation of comet Borrelly

Meemong Lee and Richard Weidner, *Jet Propulsion Laboratory*, and Laurence Soderblom, *USGS*

The rich science-return from the deep space 1 mission was enabled by several break-through technologies including autonomous optical navigation (AutoNav), miniature integrated camera and spectrometer (MICAS), on-board data processing, model-based science observation sequence planning, and science information analysis. Digital image/signal processing was a critical element of the mission for verifying the spacecraft's orientation, tracking the encounter target, calibrating the instrument, processing the data, and analyzing the observed phenomena This paper describes a few notable challenges with respect to flight calibration, on-board data processing, and science information analysis.

TPM1L-223 -- A Study of Supervised, Semi-Supervised and Unsupervised Multiscale Bayesian Image Segmentation

Xiaomu Songand Guoliang Fan, *Oklahoma State University*

In this paper, we study multiscale Bayesian image segmentation with respect to the different availability of image features. Particularly, we adopt wavelet domain hidden Markov models, i.e., HMT and HMT-3S, to obtain statistical image characterization. We also apply the joint multi-context and multi-scale (JMCMS) approach to exploit robust multiscale contextual information. We first review the supervised multiscale Bayesian segmentation algorithms where image features are given. Secondly, we study semi-supervised segmentation by only providing partial image features. The K-mean clustering is used to convert the semi-supervised segmentation problem into the self-supervised process by identifying the reliable training samples. Thirdly, an unsupervised segmentation algorithm is also developed where image feature are completely unknown and can be

trained online during segmentation. The simulation results on a synthetic mosaic show that the proposed algorithms can achieve high classification accuracy by using HMT-3S and JMCMS.

TPM1L-223 -- The Analysis of Normal Mammograms

Edward Delp, *Purdue University*

Majority of the screening mammograms are normal, and it will be extremely beneficial if a detection system is designed to help radiologists readily identify normal regions of mammograms. Therefore, it can help them focus on suspicious areas. In this paper, first we will present a binary decision tree classifier constructed from normal and abnormal regional images. This decision classifier is then applied to the background-removed whole mammograms for normal classification by using moving block scheme. This is fundamentally different than other approaches, which identify normal mammograms by detecting a certain type of cancer. Our approach presented here is independent of the types of the abnormalities.

TPM1L-223 -- Automatic Assessment of Fabric Smoothness

Christopher Turner, Hamed Sari-Sarraf, Aijun Zhu, Eric Hequet, and Sunho Lee, *Texas Tech University*

Due to its direct impact on the aesthetic appeal of apparels, a fabric's propensity to wrinkle is one of its most important characteristics. As such, access to a quantitative method of assessing fabric smoothness is of the utmost importance to the textile community. In this paper, we describe a vision system for measuring fabric smoothness in terms of its image acquisition and analysis modules. The acquisition module is a laser-based surface profiling system that utilizes a smart CMOS camera to sense the 3-D topography of the fabric specimens. The image analysis module is comprised of methods based on anisotropic diffusion and the facet model for characterizing the different edge information that ultimately relate to a specimen's degree of wrinkling. Promising preliminary results will also be included.

TPM1L-225 -- Power Electronics I

Tuesday: 2:00 pm– 3:20 pm

Chair: Kaveh Ashenayi

University of Tulsa

TPM1L-225 -- Introduction of Power Electronics to Electric Machines Lab

Swakshar Ray, Seungwon An, and Thomas Gedra, *Oklahoma State University*

This paper presents a proposal for a new upgrade that will incorporate power electronics experiments in the electric machines lab at Oklahoma State University (both Stillwater and Tulsa campuses). We will introduce a general lab setup which includes digital data acquisition (DAQ) and virtual instrumentation. The application of 3 phase inverters will be discussed with our lab setup. The installation of flexible AC transmission system (FACTS) devices in our 3-bus power system will be presented. In addition, a modelling of unified power flow controller (UPFC) for the use of optimal power flow (OPF) will be described.

TPM1L-225 -- Performance of a Fault Diagnosis Method Based on Wavelet Characterization

Masoud Karimi-Ghartemani, Hossein Mokhtari, and Reza Iravani, *University of Toronto*

This paper shows performance of a fault diagnosis method in a typical application in which fast detection of fault is necessary. The fault diagnosis method is based on characterizing the signal features using wavelet transform. The power system is a static transfer switch (STS) which requires a fast detection of the fault instant. The method is experimentally verified and compared to a conventional method. Results approve superiority of the wavelet characterization method.

TPM1L-225 -- Advance Analysis of Haar Transform-Based Control for DC Motors

Alexander Ageyev, *Seversk State Institute of Technology*, Alessandro Gandelli and Sonia Leva, *Politecnico di Milano*

A more careful analysis on the system formed by a dc motor fed by a chopper is performed in this work thanks to a more sophisticated mathematical apparatus. Previous mathematical analysis has been conducted through Haar functions in order to establish bases for a reliable and efficient real time control of chopper-motor systems. The tool based on the general framework of wavelets has been improved and better tuned on this specific application. A more accurate comparison of existing methods used to solve differential equations and the Haar domain techniques are presented and critically discussed. Transient conditions during the starting process and duty cycle effects can usefully be examined using such technique, putting into evidence specific characteristics of the chopper-motor system. Examples describing the application of the proposed technique are presented and critically discussed.

TPM1L-225 -- High Frequency Model of PCB-Based Three-Winding Transformer

Cesare Mario Arturi, Alessandro Gandelli, and Flavia Grassi, *Politecnico di Milano*

An equivalent network of printed-circuit-board (PCB) based three-winding transformers is presented for simulating high frequency behaviour (at some MHz). The PCB-based transformers do not require the manual winding procedure and thus simplify the manufacturing process of transformer-isolated gate drive circuits. The use of the multiple secondary outputs can simplify the complementary gate drive circuits that are often required in many power electronics applications. A systematic procedure is presented to deduce the inductive and the capacitive coupling model that can be easily extended to multi-winding transformers. The numerical evaluation of the model parameters is carried on and the frequency response of the model is discussed.

TPM1P-140 -- DSP System, Design, and Implementation

Tuesday: 2:00 pm– 3:20 pm

Chair: Mohamad Farooq

Royal Military College of Canada

TPM1P-140 -- Reduction in Hardware by Allowing Adder Sharing in Filter Coefficients

Sunil Madgula and Michael Soderstrand, *Oklahoma State University*

Savings in the hardware is better achieved by reducing the number of adders required to perform the shift and add multiplication used in the filter coefficients. A new method of reducing the hardware complexity in designing a transposed direct form filter is investigated and the reduction in the costs by this method is presented.

TPM1P-140 -- Arctan Differentiated Digital Demodulator for FM/FSK Digital Receivers

Haitham Eissa, *Mentor Graphics*, Khaled Sharaf and Hani Ragaie, *Ain Shams University*

In this paper a new FM/FSK digital demodulator based on the digital ARCTAN algorithm, is proposed. The proposed digital FM/FSK demodulator is called ARCTAN Differentiated demodulator. The demodulator is based on quadrature Q & I signals. Direct division of quadrature signals rejects amplitude modulation components. The proposed demodulator works for both narrow & wide band FM/FSK signals. The demodulator is shown to be suitable for integration in digital FM receivers.

TPM1P-140 -- Restrained Neighborhood Analog Median Filters

Alejandro Diaz-Sanchez, *National Institute for Astrophysics, Optics and Electronics*, and Jaime Ramirez-Angulo, *New Mexico State University*

The implementation of highly parallel median filters for image processing using a reduced interconnection complexity is presented. The performance of the noise removal process is analyzed, and the results are compared with the previously reported. Two analog median filters were used with this technique: a median filter

that is based in a transconductance comparator, and a subthreshold operation median filter. Simulation results of a 78 X 89 image corrupted, with 15% salt and pepper noise, are shown. All the simulations were made using BSIM3 level 49 model and 1.2 ƒÝm MOSIS parameters

TPM1P-140 -- Analysis and Enhancements for EBCOT in High-Speed JPEG2000 Architectures

Yijun Li, Ramy Aly, Beth Wilson, and Magdy Bayoumi, *University of Louisiana at Lafayette*

Due to the advanced features of the JPEG2000 compression algorithm, hardware designs of the system often face great challenges in terms of reducing delay, power, and silicon area. This paper implements an architecture for Tier-1 of EBCOT in the JPEG2000 encoder that focuses on high speed. Through the design process, critical components that affect the speed of the system are identified and enhancements to reduce the delay are presented at the system and circuit levels. Simulations results show a 17% improvement in speed for some of these components.

TPM1P-140 -- Improved Numerically Controlled Digital Sinusoidal Oscillator

Shubhada Deo, Sreeraj Menon, Saritha Nallathambhi, and Michael Soderstrand, *Oklahoma State University*

The design of a digital sinusoidal oscillator with finite word length having excellent capability to reduce DC drift, frequency and amplitude drifts is proposed. The design utilizes the fundamental properties of a simple second order difference equation. The key element of this NCO is a ROM look-up-table (LUT) that translates the control input into a value of beta (the cosine of the desired frequency angle theta) that guarantees stability of the oscillator. The disadvantage is that the frequency of oscillation may be slightly different from that specified by the NCO input. But the result is an oscillator that has zero drift in amplitude, DC value or frequency. The proposed oscillator utilizes an LUT, a single multiplier, two input adders and two delays. Simulations confirm the no DC drift, no amplitude distortion and no frequency drift occur for long-term oscillation.

TPM1P-140 -- Fast Prototyping of a DSP Core

Mehdi Fakhraie, *University of Tehran,* Mohammad Tehranipour, *University of Texas at Dallas,* Mohammad Movahedin, *University of Tehran,* and Mehrdad Nourani, *University of Texas at Dallas*

This paper describes the UTS-DSP (University of Tehran and SAMA Recearch Center) IC design process. Using CISC architecture, UTS-DSP has an efficient pipeline to cover a complete instruction set as a high-performance DSP processor. This paper has mainly focused on major parts of UTS-DSP design process, modeling and verification as a fast and efficient process to design DSP cores. Modeling of the UTS-DSP is done by VHDL hardware description language and then synthesized for test implementation via FPGAs. A dedicated hardware has been developed for FPGA implementation with 250,000 logic gates and over five million memory bits.

TPM1P-140 -- Echo Cancellation in IP networks

Zeljko Zilic, *McGill University,* Jan Radecki, *Technical University of Szczecin,* and Katarzyna Radecka, *McGill University*

Voice transmission over IP network imposes new DSP challenges. Package loss and a latency caused by packets buffering have an essential influence on the speech quality. These features have also an impact on the line echo canceller (EC) performance. The constant latency usually greater than 60 milliseconds causes that an echo is very well audible even for a short echo path delay. Therefore, the EC must be deployed on each 2-wires/4-wires connection while on a conventional transmission only toll connections require EC. Large total delay requires short convergence time and big echo return loss enhancement. The package loss is related to non-stationary intervals of speech which results in requirements for good EC performance in tracking statistical variations of the signal. The IP networks need more robust and inexpensive EC than conventional networks. In this paper we address issues related to the EC for IP networks.

TPM1P-140 -- Hardware Efficient Narrow Band FIR Filter

Vivek Venugopal, Khalid Abed, Raymond Siferd, and Shailesh Nerurkar, *Wright State University*

Abstract-This paper presents a novel approach to implement a narrow band Finite Impulse Response (FIR) digital filter that requires less hardware than traditional FIR filter implementations. The hardware efficient Canonic Signed Digit (CSD) multiplier is used instead of the conventional multiplier to reduce the hardware. The digital filter has been initially designed using Simulink, DSP Blockset and has been tested for the required frequency response using Matlab. The FIR filter has been modeled and verified using Verilog HDL and is implemented using FPGA Xilinx 4000 technology. The use of the multistage multirate approach for the design of the FIR filter stages results in a hardware saving of about 80%.

TPM1P-140 -- DSP for RFID

John Engel, *Boeing*

A synthesized hardware circuit is being developed, using embedded software in a Digital Signal Processing (DSP) Chip. This design recovers the minute signals, which are subject to interference from a passive H-field Radio Frequency Identification (RFID) device. This design increases the range of detection, while reducing the read time and false readings.

TPM1P-140 -- Design Methodology for Broadband Delta-Sigma Analog-to-Digital Converters

Mona Safi-Harb and Gordon Roberts, *McGill University*

A systematic method for designing broadband delta-sigma modulators will be described. In particular, we shall describe the design of a delta-sigma modulator in a 0.18 Micron CMOS process achieving a 13 bit resolution over a 1 MHz bandwidth. Circuit non-idealities in the main building blocks are modeled in Simulink/Matlab allowing one to optimize the design for power, bandwidth and resolution. Methods for enhancing the speed of optimization will be described.

TPM1P-140 -- Multiple Description Image Coding Using Pixel Interleaving and Wavelet

Longji Wang, Srikanta Swamy, and M. Omair Ahmad, *Concordia University*

Multiple description coding encodes a source image into two or more mutually refinable bitstreams to overcome channel impairments. When one or more channels fail, received bitstream(s) are decoded to provide a lower but acceptable quality of the reconstructed image. This paper proposes a multiple description image coding scheme using pixel interleaving by taking advantage of the intrinsic correlation of the adjacent pixels. We improve substantially the performance of the reconstructed image from multiple descriptions by compromising to some extent the performance of the reconstructed from a single description. This is achieved by incorporating the wavelet transform into the pixel interleaving-based encoder so as to provide the ability to trade off the quantizations of the frequency coefficients and the spatial pixels. Simulations are presented to demonstrate the effectiveness of the proposed schemes.

TPM1P-140 -- A Recursive Approach to the Design of Linear-Phase Half-Band Digital Filters Having Very Sharp Transition Bands

Nan Li and Behrouz Nowrouzian, *University of Alberta*

Linear-phase FIR digital filters having sharp transition bands find a wide variety of applications in modern digital signal processing. By using the conventional techniques, the resulting FIR digital filters require a large number of taps, making their hardware implementation expensive. This paper presents a recursive approach to the design of linear-phase half-band digital filters having very sharp transition bands. It is shown that by embedding a half-band filter between proper decimation and interpolation stages, one can make the filter transition band sharper. In this way, a half-band digital filter having very sharp transition band can be realized recursively, by starting from a half-band filter with very gradual transition band. The required sharpness can be achieved by increasing the number of recursions.

TPM2L-209 -- Image Sensors
Tuesday: 3:40 pm– 5:00 pm
Chair: Franco Maloberti
University of Texas at Dallas

TPM2L-209 -- Design of an Analog Ranking System Using Optical Intensity Comparison Smart-Pixels with Programmable Intensity Offset Levels

Fred Beyette and Rajsekhar Aikat, *University of Cincinnati*

This project involves the design and simulation of a smart-pixel arrangement capable of compensating the interconnect losses of two analog optical signals based on its positional coordinates in the wave-guide array and a programmable attenuation factor, before comparing them to produce a digital output. This pixel has been incorporated into an optical co-processor system to rank an array of analog optical signals, with an operation time almost independent of the number of inputs.

TPM2L-209 -- A Wide Dynamic Range CMOS Digital Pixel Sensor

Jean-Luc Trepanier, Mohamad Sawan, Yves Audet, Jonathan Coulombe, *Ecole Polytechnique Montreal*

A CMOS image sensor with pixel level analog to digital conversion is presented. Each 13.8µm x 13.8µm pixel area contains a photodiode and a dynamic comparator using the maximum voltage swing available (0V - 1.8V). The comparator does not need any bias current and is insensitive to fabrication process variations. Also a digital to analog converter (DAC) is used to deliver a voltage reference in order to compare it with the pixel voltage for the analog to digital conversion. This DAC provides the possibility to convert the pixel voltage linearly or to compress it logarithmically. The circuit allows image captures at multiple exposure times, and the resulting values are delivered in floating digital format, offering the possibility to expand the intrascene dynamic range to more than 84 dB. The circuit was implemented in a CMOS 0.18µm process and has been submitted for fabrication.

TPM2L-209 -- A Color Image Sensor Using Adaptive Color Pixels

Wei Jean Liu and Oscal T. -C. Chen, *National Chung Cheng University*, Li-Kuo Dai, Ping-Kuo Weng, Kaung-Hsin Huang, and Far-Wen Jih, *Chung-Shan Institute of Science & Technology*

A color image sensor using adaptive color pixels is proposed where the adaptive color pixel is based on three PN junctions to sense color spectrum. The three PN junctions from four layers of which junctions are selected by two control signals to get RGB photo responses on the same pixel. In actuality, such approach could effectively replace the color filter process commonly used today in color image sensors.

TPM2L-209 -- Design of a 32 by 32 Read Head device for Page-Oriented Optical Memory

Hang Li and Fred Beyette, *University of Cincinnati*

In this paper, the concept of page-oriented reading for the next generation optical storage devices is introduced. The design of a read head device that is capable of simultaneously reading a page of 32 by 32 bit optical data is conceived. The feasibility of the design is analyzed, presented along with the current progress in implementing the entire system.

TPM2L-211 -- RF and Microwave Amplifiers and Mixers II

Tuesday: 3:40 pm– 5:00 pm

Chair: Danny Pinckley

Motorola

TPM2L-211 -- A Merged Variable Gain CMOS LNA and Sub-harmonic Mixer for a 2-GHz Direct Conversion WCDMA Application

Kwang-Jin Koh, *Electronic Telecommunication Research Institute*

A merged LNA and sub-harmonic mixer is proposed for a 2GHz WCDMA DCR application. It adopts differential variable gain LNA to increase system dynamic range and 2nd order linearity. To remove DC offset, which can be introduced by self-mixing problem, the proposed architecture uses sub-harmonic mixing technique. To increase LO to RF isolation, we use 0.18ìm triple-well CMOS process. The system shows 30.5dB and 22dB conversion gain at high gain mode and low gain mode respectively. In each case, the IIP2s are 26dBm and 46dBm, and IIP3s are –14dBm and –1.5dBm. The overall power consumption is less than 18mW. All circuit simulations are based on 0.18 ìm CMOS technology with 1.8V supply voltage

TPM2L-211 -- A Merged RF Front-end Design for a 2GHz WCDMA DCR Application

Kwang-Jin Koh, *Electronic Telecommunication Research Institute*

A merged variable gain differential CMOS LNA and mixer is proposed for a 2GHz WCDMA DCR application. Variable gain stage is placed before frequency down-mixing stage to increase system dynamic range. To increase LO to RF isolation, thus to overcome DC-offset problem, we use 0.18ƒÝm triple-well CMOS process. The system shows 27.5dB and 19dB conversion gain at high gain mode and low gain mode respectively. In each case, the IIP2s are 22dBm and 32dBm, and IIP3s are ¡V14.8dBm and ¡V4.3dBm respectively. The overall power consumption is less than 18mW. All circuit simulations are based on 0.18ƒÝm CMOS technology with 1.8V supply voltage

TPM2L-211 -- A 1V CMOS Power Amplifier for Bluetooth Applications

Ka Wai Ho and Howard Cam Luong, *The Hong Kong University of Science and Technology*

A two-stage power amplifier operated at 2.4GHz has been designed and fabricated in a standard 0.35mm CMOS technology. A common-gate Class E power amplifier is employed. A common-gate switch is suitable for low supply voltage operation without degrading the PAE. A pre-amplifier with positive feedback configuration is used to drive the common-gate output stage. The amplifier delivers 18dBm output power with 33% power-added efficiency (PAE) under a 1V supply voltage. With a 1.2V supply, the amplifier delivers 20dBm output power with 35 % PAE and can be integrated for class 1 Bluetooth application.

TPM2L-211 -- Digitally Assisted Feedforward Power Amplifier

Danny Pinckley, Thanh Chu, and Sean McBeath, *Motorola Labs*

Digitally Assisted Feedforward (DAFF) is a digital enhancement to a feedforward power amplifier (PA). In the standard feedforward configuration, both on-channel and off-channel distortion is suppressed. In the DAFF configuration, a special reference signal is generated such that only the off-channel distortion is suppressed. This process greatly reduces the peak-to-average power in the error amplifier, which facilitates an increase in output power for the entire amplification circuit. Additionally, one can suppress on-channel distortion to varying degrees, which simply reduces, to varying degrees, the improvement in output power.

TPM2L-213 -- Testing and BIST II
Tuesday: 3:40 pm– 5:00 pm
Chair: Degang Chen
Iowa State University

TPM2L-213 -- A Pseudo-random Testing Scheme for Analog Integrated Circuits Using Artificial Neural Network Model-based Observers

Prithviraj Kabisatpathy, Alok Barua, and Satyabroto Sinha, *Indian Institute of Technology*

This paper presents a simple and very efficient testing strategy for fault diagnosis of analog integrated circuits. The methodology is based on a technique of using a pseudorandom noise as the test pattern and a model-based observer for fast and robust testing and fault diagnosis. By incorporating device-level faults the efficiency is illustrated for stand-alone as well as embedded operational amplifiers as examples. The simulation results obtained are very encouraging. The technique can be viewed as a built-in self-test along with a design for testability scheme that dramatically improves the fault coverage and can be implemented for both on-line and off-line depending on the need of the application and silicon area overhead. Its main advantages are: a universal input stimulus (white noise) is used and thus test generation can be avoided, good and faulty signatures for high quality testing can be easily constructed and testing cost can be minimized, the technique is very efficient and robust, and the scheme can be well suited for built-in self-test implementation.

TPM2L-213 -- The C-testability Analyze of the SuperBlock Carry-LookaheadAdder (SBCLA)

Daniela Popescu and Corneliu Popescu, *University of Oradea - Romania*

The paper is the result of the authors?ctivities concœrning the testing and the design for testability for Computer arithmetic systems. Our already published results, together with the C-testable concept, are very important in testing other kinds of practical adders, which includes cells with CLA units. So, by applying the C-testability concept we present a method for identifying a minimal complete set of test vectors for detecting all single stuck-at faults for the Superblock Block Carry-Lookahead Adder (SBCLA)), together with our results.

TPM2L-213 -- Comparison and Analysis of Delay Elements

Nihar Mahapatra and Alwin Tareen, *University at Buffalo, The State University of New York,* and Sriram Garimella, *Andiamo Systems, Inc.*

This paper comprehensively reviews ten different delay element architectures for use in CMOS VLSI design. They can be categorized into three separate families: transmission gate based, cascaded inverter based, and voltage-controlled based. Six of these delay elements are already in use and we propose four new ones. We compare these delay elements, both analytically and using simulations, in terms of four important parameters: delay, signal integrity, power consumption, and area, and find that they have widely varying characteristics. The results presented in this paper, expressed as parameter ranges, will enable a designer to select the most appropriate delay element that meets delay, signal integrity, power consumption, and area specifications.

TPM2L-214 -- Low Power Circuits and Architectures II

Tuesday: 3:40 pm– 5:00 pm

Chair: Lex A. Akers

University of Missouri

TPM2L-214 -- Low Power and High Speed Explicit-Pulsed Flip-Flops

Peiyi Zhao, Tarek Darwish, and Magdy Bayoumi, *University of Louisiana at Lafayette*

Flip-flops play an important role in building digital CMOS designs. Their design and optimization is critical for high-performance and low power systems. In this paper, we propose high-performance and low power flip-flops based on the Explicit-Pulsed Flip-Flops (EPFF). These new flip-flops eliminate the hazardous glitches associated with the original EPFF output. The Static-EPFF is developed for low-power dissipation purposes; it reduces the power dissipation by 13.9%-15.7%, and it enhances the speed by 4.86%-7.87%. For high-speed objectives, the STC-EPFF achieves 21% enhancement in speed over EPFF at the expense of increased power dissipation (12%). Such achievements were obtained by using Static CMOS instead of dynamic CMOS. Also the setup times for both flip-flops is found to be less than that of the EPFF.

TPM2L-214 -- An Efficient Asynchronous Pipeline FIFO for Low-Power Applications

Morteza Gholipour and Ali Afzali-Kusha, *University of Tehran*, Mehrdad Nourani, *University of Texas at Dallas*, and Ahmad-Reza Khademzadeh, *Iran Telecom Research Center*

In this paper, an efficient micropipeline FIFO for low-power applications is introduced. In this FIFO, instead of using a latch in each stage, an inverter gate with a weak keeper is utilized. This leads to a significant reduction in the number of transistors and the power consumed by the circuit. To demonstrate the efficiency of the design, a 16-bit 4-stage FIFO with four-phase micropipeline control is designed using this approach and a traditional style which uses latches in each stage of the FIFO. The number of transistors is reduced more than 43 percent. The designs are then simulated using HSPICE with 0.6µm CMOS parameters. The results of the power consumption show a power reduction of more than 72 percent.

TPM2L-214 -- Switching Activity Minimization by Efficient Instruction Set Architecture Design

Rakesh Kumar, *University of California, San Diego,* V. Ramakrishna, *University of California, Los Angeles,* and Anupam Basu, *Indian Institute of Technology, Kharagpur*

Power consumption can be greatly minimized by reducing the bus signal transition activity (also called switching activity) in the control and data path circuit. Switching activity occurs due to the switching between two instructions (of the embedded software) on successive clock cycles. Our belief is that the binary encoding of instructions (machine code) plays a significant role in determining the amount of switching in a circuit. Thus, our aim is to realise a machine encoding of instructions of an ASIP such that for a given data path, it will minimize the average switching activity in the control path circuit of the ASIP and hence the total switching activity in the ASIP. Given the application-domain of the ASIP, we have used information theoretic techniques to arrive at an encoding of the op-code that minimizes redundancy and also the switching activity. We have compared our encoding of instruction op-codes with those obtained by other encoding techniques using a switching activity estimator designed by us

TPM2L-214 -- A Low-power VLSI Design of a HMM Based Speech Recognition System

Shingo Yoshizawa, Yoshikazu Miyanaga, and Naoya Wada, *Hokkaido University*

This paper reports a low-power VLSI design of a HMM based speech recognition system. Output probability calculation is the most computationally expensive part of continuous HMM (CHMM) based speech recognition. The proposed architecture calculates the output probability with parallel and pipeline processing. It enables to reduce memory access and have high computing efficiency. The novel point is the efficient use of register arrays that reduce memory access considerably compared with any conventional method. The implemented system can achieve a real time response with lower clock in a middle size vocabulary recognition task (100-1000 words) by using this technique.

TPM2L-216 -- VLSI Synthisis II
Tuesday: 3:40 pm– 5:00 pm
Chair: Mitch Thornton
Mississippi State University

TPM2L-216 -- Spectral and Two-Place Decomposition Techniques in Reversible Logic

Michael Miller, *University of Victoria*

A digital circuit is reversible if it maps each input vector into a unique output vector. Reversible circuits can lead to low-power CMOS implementations and are also of interest in optical and quantum computing. In this paper, we consider the synthesis of reversible logic assuming primitive reversible devices such as Feynman, Toffoli and Fredkin gates. In particular, we consider the use of Rademacher-Walsh spectral techniques and two-place decompositions of Boolean functions. Preliminary results are given for reversible and nonreversible functions and show that the approaches described do indeed show promise.

TPM2L-216 -- SRFCC: Synthesis of RF CMOS Circuits

Subramaniam Kaitharam, Chandrasekar Rajagopal, and Adrian Nunez-Aldana, *Syracuse University*

In this paper, we present a methodology to synthesize CMOS RF devices from high-level circuit specifications into transistor net-lists. The core of the methodology is an estimator of RF analog CMOS circuits, which evaluates the performance parameters of various circuit topologies. The estimation engine is based on a hierarchical analog performance estimator and a set of heuristics. The synthesis environment considers all performance parameters into account, and it relies on a genetic algorithm based heuristic method to search for a solution in a large design-space. The synthesis tool determines a solution set of design parameters such that the RF circuit satisfies the overall design constraints.

TPM2L-216 -- Computer Tools for Switched-Current Filter Design

Andrzej Handkiewicz, *Poznan University of Technology*

The paper is devoted to design automation of switched-current (SI) filters. Three computer tools were elaborated recently by the authors. Two of them are useful at the stage of behavioral synthesis for symbolic analysis and design of a lossless prototype circuit. The third program, for layout generation of current mirrors, can be used for silicon assembly of an SI filter. In the presented synthesis method current mirrors are basic parameterized cells of such filters. The current mirrors are composed of transistors which width-to-length ratios of channels are determined at the behavioral synthesis stage of the filter.

TPM2L-216 -- Employing Layout-Templates for Synthesis of Analog Systems

Hua Tang and Alex Doboli, *State University of New York at Stony Brook*

This paper presents an original methodology for layout-aware synthesis of analog systems. Layout parasitics (including capacitance, resistance and inductance) have a critical influence on system performances i.e. speed, bandwidth etc. We discuss the usage of layout templates during an exploration-based synthesis methodology that performs combined system parameter search, floorplanning and global routing. Predefined templates express the relative position of blocks and wires so that routing parasitics can be fastly extracted and considered during synthesis. The paper also presents the selection of the best layout template from a set of possible candidates. Two case studies are presented to exemplify the usage of layout templates for synthesis.

TPM2L-218 -- Advanced Networking Systems II

Tuesday: 3:40 pm– 5:00 pm

Chair: Bon-Jin Ku

Oklahoma State University

TPM2L-218 -- Technologies and Structures to Support Remote and Virtual Lab Experiences

Mark Weiser, *Oklahoma State University*

Hands-on experience with technology is critical to ground knowledge learned in traditional higher education. Increasingly, curriculum is being made available at a distance through real-time and asynchronous video, as well as the Internet. Unfortunately, the high cost of lab equipment makes travel to a common site imperative for for students to obtain practical application on current equipment. This paper outlines a model for implementing remote interaction with lab equipment of many types and describes an functional implementation of the virtual model.

TPM2L-218 -- Comparative Study of the Firewire IEEE-1394 Protocol with the Universal Serial Bus and Ethernet

Gautam Ramamurthy and Kaveh Ashenayi, *The University of Tulsa*

This paper presents results of study of The IEEE 1394 protocol, which is the IEEE standard for a high performance serial bus with similar, and more widely used technologies like the Universal Serial Bus 1.0 and the Ethernet Protocol. A thorough theoretical and experimental investigation between the technologies is made with respect to the actual architecture of the buses and their practical applications. Experiments include setting up a small network and testing the actual data transfer speeds of the protocols. Performance of these protocols in a general teleconferencing environment was also studied.

TPM2L-218 -- Smart Packet Processor Design for the Cognitive Packet Network Router

Taskin Kocak and Jude Seeber, *University of Central Florida*

As the Internet expands significantly in numbers of users, servers, IP addresses, and routers, the IP based network architecture must evolve and change. Recently, Cognitive Packet Networks (CPN) was proposed as an alternative packet network architecture, where there is no routing table, instead reinforcement learning (Random Neural Networks) is used to route smart packets [1,2]. CPN routes packets based on QoS, using measurements that are constantly collected by packets and deposited in mailboxes at routers. Previously, CPN is implemented in a software test-bed. In this paper, we present design approaches for CPN network processor chip. Particularly, we discuss implementation details for one of the modules in the chip: The smart packet processor, which includes a neural network hardware design.

TPM2L-218 -- Analyzing End-to-End Delivery Delay in Pure VoIP Networks

George Scheets and Ritu Singh, *Oklahoma State University,* and Marios Parperis, *Williams Communications Group*

Today, standards-based Quality of Service mechanisms are not universally deployed across Internet Service Provider backbones. As a result, many carriers that are deploying VoIP networks are segregating voice traffic from the data and installing pure VoIP backbones in order to better guarantee high quality. Of particular interest is maintaining end-to-end delivery of the voice information within some time bounds. This paper examines sources of end-to-end delays associated with VoIP calls, discusses differences between fixed and variable rate coding, and illustrates how trading off packet size versus router delay can impact the number of voice calls supportable by the network.

TPM2L-219 -- Adaptive Systems II
Tuesday: 3:40 pm– 5:00 pm
Chair: Edward Wilson
Intellization

TPM2L-219 -- An Adaptive View of Timing and Synchronization

William Sethares, *University of Wisconsin*, John Walsh and C.R. Johnson, Jr, *Cornell University*

Many of the standard tasks in telecommunication systems can be viewed as optimization problems, and these can often be solved using an adaptive (gradient) style iteration. This paper shows how the synchronization tasks of timing recovery and phase tracking can be stated and solved using iterative adaptive algorithms. One of the more interesting theoretical issues comes from the incorporation of several different adaptive loops within one system. What are the interactions between the various adaptive subsystems, and how can the interactions be quantified?

TPM2L-219 -- Polymorphous Computing Applied to the Electronic Nose Architectures

Robert Ewing, *Wright Patterson Air Force Base,* Hoda Abdel-Aty-Zohdy, *Oakland University,* and James Moncrief, *Air Force Research Laboratory*

The electronic nose (enose) is applied to detect, monitor and identify a wide range of environmental organic, inorganic and biochemical vapors. Typically, airborne substances are made up of hundreds of different inorganic/organic or bio molecules. The molecules usually have properties that can be identified with different detection systems, such as gas chromatography and mass spectrometry. However, the systems are usually bulky, expensive and time consuming to be deployed portably. Recently, the growing application of polymorphous computing opened up the opportunity for the use of neural net and genetic algorithm development for electronic nose selectivity with critical information extraction methodology done in real-time. The additional use of Power Aware Computing/Communication (PAC/C) and Polymorphous Computing Architecture (PCA) enables the enose to "Tailor" power through energy management at all levels of application/system for size, weight, power, scalability, complexity and temporal and functional reconfiguration constraints.

TPM2L-219 -- Spike Delay Controllable Neuron

Robert Fujii, Gou Sase, Yoshio Konishi, and Hesham Amin, *University of Aizu*

The circuit design of an analog/digital spiking neuron with controllable spike delay is proposed. The circuits were simulated using Cadence's SpectreS simulator and BSIM3 AMI 0.6 um geometry MOS transistor parameters provided by MOSIS. The estimated static power dissipation was 280 pW for the dendrite and 56 pW for the soma. Dynamic power dissipation was approximately 11.1 pJ/dendrite input switching and 4 pJ/soma output spike switching. A spiking neural network which uses Hebbian learning is presented as an application of this type of neuron.

TPM2L-219 -- Hardware Implementation of a Low-Power Pipelined LMS Adaptive Filter

Bulent Dukel and Maher Rizkalla, *Indiana University/Purdue University*

This paper describes the implementation of a pipelined low-power 6 taps adaptive filter based on the least-mean square (LMS) algorithm. The process of the power characterization procedure is a very efficient and can be easily set in synthesis based design flows. No additional effort is required from the designer, since power characterization merges seamlessly with a natural top-down design methodology with iterative improvement.

TPM2L-221 -- Mixed Signal and Signal Conversion Processing II

Tuesday: 3:40 pm– 5:00 pm

Chair: J. W. Bruce

Mississippi State University

TPM2L-221 -- Quadrature Integral Noise Shaping For Generation of Modulated RF Signals

Pallab Midya, Poojan Wagh, and Patrick Rakers, *Motorola Labs*

This paper introduces a method to produce a modulated RF signal using a digital pulse signal switching at the carrier frequency. The entire modulation and amplification lineup is implemented in the digital domain. Integral Noise Shaping (INS) is used to create the baseband signals (I,Q) as digital PWM signals which are then mixed with a pair of digital carrier signals. All the edges of the digital pulse modulated signal line up with an edge of a fixed frequency clock signal at twice the carrier frequency. The resulting digital signal has high linearity and low quantization noise. All switching spurs and the quantization noise can be cleaned up with a bandpass filter with reasonable Q factor. Simulation results are presented for an offset tone test signal.

TPM2L-221 -- Enhancing Performance in Interpolating Resistor String DACs

Latinus Boylston Jr., *Iowa State University,* Kenneth Brown, *Honeywell Inc,* and Randall Geiger, *Iowa State University*

Several techniques for enhancing the performance of interpolating resistor string digital-to-analog converters (DAC) are discussed. These techniques will enhance both static and dynamic performance. The resulting circuit structures compensate for the inaccuracies inherent in the coupling of the interpolator to the coarse resistor string by isolating or eliminating the voltage drop across the coarse tap selection switch.

TPM2L-221 -- Adaptive Design Method for Efficient Direct Digital Synthesis

J.W. Bruce, J.E. Creekmore, S.R. Porter, and R.P. King, *Mississippi State University*, and B.J. Blalock, *University Tennesse-Knoxville*

In this paper, an area and power efficient ROM-less DDFS circuit with sinusoidal output is proposed. Sinusoidal spaced reference voltages are generated using an integrated resistor with a complex geometry. The DDFS accumulator output controls the nonlinear sinusoidal DAC directly and without the power-hungry ROM. The proposed design is independent of sheet resistance, and voltage reference power dissipation can be tailored to the application. Photolithography limitations can introduce geometry errors, thus, reference voltage errors. An adaptive design algorithm is proposed that reduces reference errors by more than an order of magnitude compared to the original design. Finally, a CMOS implementation of the proposed DDFS architecture is presented.

TPM2L-221 -- A Dynamic Element Matching Approach to ADC Testing

Beatriz Olleta, Degang Chen, Randall Geiger, *Iowa State University*

A dynamic element matching approach to ADC testing is presented. With this technique a highly nonideal DAC is used to generate an excitation to the DUT. Dynamic element matching is used to create a statically precise excitation from imprecise components. Simulation results show this approach can be used to accurately measure the performance of an ADC. This technique offers potential for use in both production test and BIST environments.

TPM2L-223 -- Signal and Image Analysis II
Tuesday: 3:40 pm– 5:00 pm
Chair: Joe Havlicek
University of Oklahoma

TPM2L-223 -- Insitu Chlorine Detection by UV Spectroscopy

Christopher Cassidy, *Sciperio,* Keith Teague, *Oklahoma State University,* Kenneth Church and Robert Taylor, *Sciperio*

A low cost spectrographic based sensor with real-time data collection and digital signal processing (DSP) for the insitu measurement of aqueous chlorine is presented. Through the use of a parallel spectrophotometer, comprised of a Xenon light source, flow-through sample chamber, spectrograph with Photodiode Array (PDA), and a DSP, frequency domain chlorine signatures are collected and processed. Data sets, of varying concentration values, are referenced to a commercially available colorimeter for evaluation of sensor performance. Based on these results and the physical properties of aqueous chlorine, calculations of the theoretical range and sensitivity Vs. optical path length (OPL) are provided.

TPM2L-223 -- A New Simplified Quantization Rate-Distortion Model for Fast Document Image Segmentation

Yan Dong, Lijie Liu, Xiaomu Song, and Guoliang Fan, *Oklahoma State University*

Document image segmentation plays an important role in compound document compression. Document image segmentation considering the rate-distortion (RD) characteristics usually outperforms the traditional segmentation approaches in terms the performance of document image compression. However, the RD model usually cannot be obtained explicitly or directly. In this paper, we will develop a simplified quantization RD (SQRD) model for fast document image segmentation. The proposed SQRD fits the multiscale Bayesian segmentation framework. The simulation results show that the new SQRD model is very promising for advanced and efficient document image analysis.

TPM2L-223 -- Defect Clustering and Classification for Semiconductor Devices

Bijoy Kundu, K Preston White, and Christina Mastrangelo, *University of Virginia*

In the semiconductor manufacturing industry cracks, breaks, scratches, contaminants, process variations, and errors by operators or equipment are all production problems that cause defects in wafers. The profitability of a manufacturing enterprise is directly tied to identifying and correcting malfunctioning processes and to learning and improvement based on past experiences. Clearly, it is highly desirable to find and classify defect signatures recorded in the test data sets and to correlate these signatures with causal data residing in the corresponding process and engineering data sets. In the first part of this paper, we seek to explore the first of these issues—automating the identification of defect clusters on individual wafers within and across lots. For that, we have developed a Visual Basic GUI and interfaced with SAS for automated clustering of defects on wafers. The selection of the right number of clusters is achieved by incorporating the Calinsky and Harbasz (CH) index. This index is calculated for increasing number of clusters and the first number of clusters for which the CH index shows a local maximum is chosen as the appropriate number of clusters. We observe, that the single-link clustering algorithm works the best in detecting the right number and shape of defect clusters [1]. In the second part of this paper, we attempt to classify these clustered defect patterns using an analytical tool used for Visual defect metrology (VDM). VDM is an in-line process monitoring technique used to assess process capability. Pattern recognition algorithms can be incorporated into visual defect metrology systems to improve process control. In this paper, we incorporate one of the pattern recognition algorithms proposed by Cunningham and MacKinnon [2] to identify scratch defects on semiconductor wafers. We apply the algorithm called the Hough Transformation (HT) to identify the scratch defect clusters generated by the clustering algorithms and observe that HT works well in detecting all kinds of scratches namely diagonal scratches (45 and 135 degrees inclination) and line scratches (both horizontal and vertical). HT has certain drawbacks which is also discussed in this work. As a part of future work, we will use neural networks and other data mining techniques such as

Discriminant Analysis, Principal Component Analysis for supervised classification of the defect clusters generated by unsupervised clustering techniques.

TPM2L-223 -- Efficient Unsupervised Estimation of Second-Order B-Spline Contour Descriptors

Tarek El Doker and Phillip Mlsna, *Northern Arizona University*

A novel unsupervised algorithm is presented for efficient and global computation of periodic second-order B-spline approximations to closed boundaries. Key local geometric information is extracted from a smoothed version of the boundary. This local information allows intelligent partitioning of the boundary and construction of an initial system of equations that often produces a very good approximation. Additional equations are introduced as local constraints to control occasional violations of the user-specified absolute error tolerance. The overdetermined systems of equations are solved by a standard least-squares approach. Computational complexity is compared to two previous algorithms. Experimental results are also provided.

TPM2L-225 -- Power Electronics II

Tuesday: 3:40 pm– 5:00 pm

Chair: Kaveh Ashenayi

University of Tulsa

TPM2L-225 -- Fuzzy Logic Control of an Active Power Line Conditioner

Phumin Kirawanich and Robert M. OConnell, *University of Missouri-Columbia*

A fuzzy logic controller for an active power line conditioner (APLC) is described. MATLAB simulations show that the proposed APLC can improve the total harmonic distortion and power factor during both steady-state and transient operating conditions.

TPM2L-225 -- Efficiency of an Active Power Line Conditioner

Chih-Jung Huang and Robert OConnell, *University of Missouri-Columbia*

The purpose of this paper is to determine the efficiency of a specific active power line conditioner (APLC) system. The APLC is a type of active filter, which cancels line current harmonics caused by nonlinear loads, by injecting a compensation current. However, because of the presence of semiconductor switching devices in the APLC, the switching and conduction losses need to be considered. Computer simulations for two load current test cases illustrate the trade-off between circuit efficiency and performance as switching frequency increases.

TPM2L-225 -- Current-Sensing Techniques for DC-DC Converters

Hassan Forghani-zadeh and Gabriel Rincon-mora, *Georgia Institute of Technology*

Current sensing is one of the most important functions on a smart power chip. Conventional current-sensing methods insert a resistor in the path of the current to be sensed. This method incurs significant power losses, especially when the current to be sensed is high. Lossless current-sensing methods address this issue by sensing the current without dissipating the power that passive resistors do. Six available lossless current sensing techniques are reviewed. A new scheme for increasing the accuracy of current sensing when the discrete elements are not known is introduced. The new scheme measures the inductor value during the DC-DC controller startup.

TPM2L-225 -- Unified Energy Conversion, Power Systems and Power Electronics Lab

Seungwon An, Swakshar Ray, and Thomas Gedra, *Oklahoma State University*

This paper introduces an unified laboratory consisting of power Systems, power electronics and energy conversions at Oklahoma State University-Tulsa. It presents more on digital data acquisition (DAQ), and virtual instrumentation (VI), the base of our unified lab. The general design of the lab setup will be described here, and

the unique designs of front panels and motor mount will be discussed in detail. Some features of virtual instrumentation are shown with real-time phasor display of AC data and spectral analysis. We can also implement power system experiments as an added feature. It concludes with a proposal for introducing power electronics using our lab setup.

TPM2P-140 -- Signal Processing
Tuesday: 3:40 pm– 5:00 pm
Chair: Tran Thong
Oregon Graduate Institute

TPM2P-140 -- Tracking Drifting Interferences Using Simple Casdaded Second-Order FIR Filters

Seng Kong, Soo Chua, and Michael Soderstrand, *Oklahoma State University*

Tracking multiple sinusoids using Kwan-Martin¡¯s algorithm is a popular approach but suffers from convergence problems due to the use of IIR filters for the notch or bandpass stages. By replacing each IIR filter with a simple FIR 2nd-order notch filter and slaving the IIR filters to these 2nd-order filters, many of the convergence problems can be solved. Using this approach a three-notch system using Grey-Markel Notch filters is able to resolve three different signals separated by 6 degrees at various locations on the unit circle.

TPM2P-140 -- Narrow-Band Interference Rejection in DS CDMA Communications Using an Adaptive IIR Notch Filter

Aloys Mvuma, *Hiroshima University,* Shotaro Nishimura, *Shimane University,* and Takao Hinamoto, *Hiroshima University*

Suppression of narrow-band interference (NBI) in direct-sequence code-division multiple access (DS CDMA) system using a lattice-based adaptive infinite impulse response (IIR) notch filter is studied. A simplified normalized coefficient update algorithm that requires no gradient signal generating filter is proposed. Convergence behaviour of the algorithm is shown not to vary much with the number of users for a tone NBI model. Closed form expression for the SNR improvement at the pseudonoise (PN) correlator input is derived. Computer simulations are shown to verify the analysis and compare the performance of the proposed NBI suppression scheme with linear predictor.

TPM2P-140 -- Transform for Continuous Time System Modeling

Tran Thong, *OGI School of Science and Engineering/OHSU,* and James McNames, *Portland State University*

In the modeling of continuous time systems, there is a need to convert the analog system to a discrete time system. The transform frequently encountered in the literature is the impulse invariant transform. This transform has proven to be inadequate for biological system modeling. In this paper we will review the available linear transforms and derive three new transforms, namely the centered step invariant transform, the local cubic spline invariant transform, and the scaled impulse invariant transform.

TPM2P-140 -- Adaptive Time Delay Estimation with Noise Suppression for Sinusoidal Signals

H. C. So, *City University of Hong Kong*

A least mean square algorithm is devised for time delay estimation between noisy sinusoidal signals received at two spatially separated sensors. Two adaptive finite impulse response (FIR) filters whose coefficients are samples of a sine function are used for delay modeling as well as noise suppression. The convergence behavior and variance of the estimated delay are also derived. Computer simulations are presented to validate the theoretical derivations of the proposed estimator for static and linearly varying delays.

TPM2P-140 -- Nonlinear Reconstruction of Oversampled Coarsely Quantized Signals

Tran Thong, *OGI School of Science and Engineering/OHSU,* and James McNames, *Portland State University*

In the course of collecting real signals, one occasionally is faced with a coarsely quantized signal. In this paper the problem of reconstructing a coarsely quantized signal using a Savitsky-Golay filter coupled with a nonlinearity is discussed.

TPM2P-140 -- Blind Source Recovery using an Adaptive Generalized Gaussian Score Function

Khurram Waheed and Fathi Salam, *Michigan State University*

The paper discusses the State Space Natural Gradient Blind Source Recovery (BSR) for minimum phase and non-minimum phase mixtures of multiple source distributions using an adaptive score function. This proposed parametric score function is derived from the generalized gaussian distribution model. An adaptive algorithm to determine the tuning parameter for the proposed score function using the batch kurtosis of BSR output is also presented. The primary advantage of the proposed framework is that it renders the adaptive estimation of the demixing network to be completely blind. No a priori information about the distribution structure of the the original sources is required. Simulation examples applying the proposed framework are also presented.

TPM2P-140 -- State Space Blind Source Recovery of Non-Minimum Phase Environments

Khurram Waheed and Fathi Salam, *Michigan State University*

The paper describes the use of the state space and the natural gradient for the demixing of sources mixed in a non-minimum phase convolutive environment. Non-minimum phase implies that some or all of the zeros of the mixing environment lie outside the unit circle, and as such the theoretical inverse or the requisite demixing system becomes unstable due to the presence of poles outside the unit circle. These unstable poles are required to cancel out the non-minimum phase transmission zeros of the environment. In order to avoid instability due to the existence of these poles outside the unit circle, the natural gradient algorithm may be derived with the constraint that the demixing system is a double sided FIR filter, i.e., instead of trying to determine the IIR inverse of the environment, we will approximate the inverse using an all zero non-causal filter. The use of the state space warrants that the derived framework is rich in structure while at the same time compact in representation. This results in derivation of update laws that can invariably handle most mixing scenarios. A simulation illustrating the performance of the algorithm is also provided.

TPM2P-140 -- Delay and Doppler Estimation Using Cyclostationarity Based Cross Correlation in a Multipath Environment

Min Yi, Ping Wei, and Xian-Ci Xiao, *UESTC,China,* and Heng-Ming Tai, *University of Tulsa*

Cyclostationarity based cross correlation delay estimation is known for its substantial tolerance to noise and interference. The multipath echoes of a transmitted signal presented at the receiver, which are not similar to noise and interference, hamper the delay and Doppler estimation from the reflection of the moving target. Thus, suppression of the multipath signals is necessary. In this paper, a cyclostationarity based multipath suppression technique is presented. An example is illustrated to demonstrate its advantage.

TPM2P-140 -- Signal Integrity Improvement in the TMDS link at UXGA

Ajinder Singh and Micheal Parten, *Texas Tech University,* and Willy Massoth, *Texas Instruments - Connectivity Group*

Transition Minimized Differential Signaling (TMDS) link connecting a Digital Visual Interface (DVI) compliant Transmitter and Receiver between a PC and a Display Device was characterized at 162MHz that is the UXGA pixel clock frequency. The transmission line model of the link was simulated using pspice and was observed from the simulation data as well as the data collected from bench that a source termination at the transmitter end in addition to the far end termination at the receiver improved the signal integrity. The improvements were seen in the eye integrity at the receiver with considerable reduction in data dependent jitter. Currently the DVI Revision 1.0 does not specify the requirement of a source termination

WAM1L-209 -- Analog Filters I
Wednesday: 9:00 am– 10:20 am
Chair: Jin Liu
University of Texas at Dallas

WAM1L-209 -- A Compact Biquadratic gm-C Filter Structure for Low-Voltage, High Frequency Applications
Armin Tajalli and Mojtaba Atarodi, *Sharif University of Technology*

A compact new biquadratic gm-C structure is developed to design low voltage, low power, and high frequency continuous-time filters. This architecture is proper for modern deep sub-micron CMOS process with limited supply voltage. Also proper Q-enhancement technique is introduced to feasibilitate the implementation of high-Q stages. One of the advantages of this technique is the independence of cutoff frequency tuning from Q-tuning. Simple architecture of the proposed biquadratics filter makes it useful for high frequency applications with proper dynamic range. Based on new biquadratic architecture, a single 1.8 V supply, low-pass, sixth-order elliptic filter in a 0.18 um CMOS process is realized. The cutoff frequency of this filter is 33 MHz and has a THD of –40 dB for 0.2 Vpp, 8 MHz signal with OIP3 of 4 Vpp. The filter consumes 1.2 mA and has 1.1 mVrms total noise.

WAM1L-209 -- Low-Distortion Continuous-Time Integrated Filters for Low
Haibo Fei and Randall Geiger, *Iowa State University*

A technique for designing high-linearity continuous-time integrated filters for low frequency applications using transconductance network is presented. With this technique, an area-efficient transconductance network is used to replace the large resistors in low-frequency integrator-based continuous-time filters. The key challenge with this technique is in determining and realizing the appropriate relationship between the transconductance circuit and the nonideal frequency-dependent properties of the opamp. Simulation results for a third-order Bessel low-pass filter designed in a 0.5u CMOS process with a cutoff frequency of 5 KHz provide a THD in excess of 70 dB for a 2V p-p output with the 5 V power supply.

WAM1L-209 -- The Design and Implementation of a Bandpass GM-C Filter for Bluetooth
Ayman Abd ElAziz, Khaled Sharaf, Hassan ElGhitani, and Hani Ragai, *Ain Shams University*

In this paper, the design of a 14th order Bandpass filter intended for low IF receiver (Bluetooth) is presented. The designed filter is fabricated in 0.6ìm CMOS DP 3M process. Measurements showed that the filter has 1.08MHz bandwidth, achieves 40dB stopband attenuation, and consumes 2.4mA from a 2.5V supply.

WAM1L-209 -- Transadmittance Type Multifunction Filter Without Using External Passive Elements
Shahram Minaei, *Dogus University*, and Oguzhan Cicekoglu, *Bogazici University*

In this paper a new transadmittance-mode multifunction filter using opamp compensation poles is presented. The proposed circuit is composed of two internally compensated operational amplifiers (OAs) and four single-output operational transconductance amplifiers (OTAs), without using external passive elements. The proposed multifunction filter can realize lowpass, bandpassand highpass responses simultaneously all at high output impedances. No matching condition is required. The circuit is suitable for monolithic implementation either with CMOS or bipolar technologies. All of active sensitivities are low. The performance of the circuits are tested using SPICE simulation program.

WAM1L-211 -- Microwave Devices and Materials
Wednesday: 9:00 am– 10:20 am
Chair: James West
Oklahoma State University

WAM1L-211 -- Meta-Materials Concepts in High-Frequency Applications
Mike Wilhelm, Robert M. Taylor, and Kenneth H. Church, *Sciperio, Inc.*

The electronics world has continued to push for reduction of physical size in terms of individual components and total package dimensions. In most cases, this size reduction has been accomplished without sacrificing quality or functionality. Conversely, the radiating structures from which many of these electronics packages will send or receive signals has not kept pace with the overall trend of reduction in physical size. Now, however, the application of meta-material concepts to high-frequency radiating structures and the substrates supporting these structures is enabling a reduction in the physical size of these elements. The size reduction is being accomplished without degradation of element performance; in some cases, it has enabled enhanced characteristics. A comparison between reduced-size structures and their traditional counterparts is presented.

WAM1L-211 -- Improving Large-Signal FET/HEMT Model Accuracy by Optimization of Diode Response
Jessi Johnson and Rick Branner, *University of California, Davis*

In this paper, a simple technique for measuring and modeling the response of the gate-source and gate-drain diodes in a large-signal FET/HEMT model is presented. Measurements are conducted on an ATF36163 PHEMT transistor, and significant improvement in a large-signal model for the PHEMT is achieved by optimizing the response of the diode models. The significance of the gate-source and gate-drain diodes in large-signal modeling is discussed.

WAM1L-211 -- SOI Implementation of Novel Triangular Layout Structures for Microwave Power Transistor Applications
Steven Morris, *Oklahoma State University*, Jie Wen, *Motorola*, Chris Hutchens and Salsbury Ryan, *Oklahoma State University*

A novel layout scheme for MOS microwave power transistors based on a triangular unit cell was implemented in silicon on insulator (SOI) technology. The triangular cell layout significantly reduces gate resistance, Rg, and source resistance Rs, when compared to multi-finger large transistors of equivalent size, leading to large gains in current gain bandwidth product, ft, and unity power gain bandwidth, fmax. Large PMOS and NMOS devices varying from 435 micron to 2237 micron channel width were implemented using Peregrine?s half micron UTSiÒ process. On-wafer s-parameter test data was acquired and equivalent circuits were derived. Data analyis was hampered by unexplained spurious resonances which are currently under investigation, otherwise measured frequency characteristics of the test transistors are near the limits imposed by the process.

WAM1L-211 -- Design of a CMOS 1.8V Low Voltage Differential Signaling Receiver
Miguel Aguirre and Carlos Heredia, *University of Puerto Rico,* Hector Torres, *Texas Instruments*, Rogelio Palomera and Manuel Jimenez, *University of Puerto Rico*

The design of a 1.8V LVDS receiver operating at a maximum speed of 700Mbits/sec is presented. The receiver is designed to accept LVDS signals from 3.3V, 2.5V, or 1.8V systems and converts it to a 1.8V digital data. The design was completed on a 0.24µm CMOS process and complying with the industry standard of ±10% power supply variations over a temperature range from -40 C to +85 C. At the nominal supply voltage of 1.8V and operating at maximum speed the receiver consumes less than 6.5mW.

WAM1L-213 -- Optical Circuits and Systems I
Wednesday: 9:00 am– 10:20 am
Chair: Sherif Michael
Naval Postgraduate School

WAM1L-213 -- Application of the SILVACO / ATLAS Software Package in Modeling and Optimization of State-of-the-Art Photovoltaic Devices
Sherif Michael, *Naval Postgraduate School,* and Panayiotis Michalopoulos, *Hellenic Navy*

A new method for developing a realistic model of any type of solar cell is presented. This is a valuable tool, considering the high cost of research and experimentation involved with the development of advanced cells. A model of an InGaP/GaAs multi-junction solar cell is prepared and is fully simulated. The major stages of the process are explained and the simulation results are compared to published experimental data. The flexibility of the proposed methodology is demonstrated and example results are shown throughout the whole process.

WAM1L-213 -- Non-contact Temperature Control in a Direct Write Laser Processing System
Nathan Kiner, *Sciperio,Inc.,* Keith Teague, *Oklahoma State University,* and Kenneth Church, *Sciperio, Inc.*

A system for coupling an infrared photodiode into the optical path of a high power CO2 laser is discussed. Through the use of an infrared sensor, an Acousto-Optical (AO) modulator, and a microcontroller based control system the temperature of the laser's target can be monitored and controlled in real time. This temperature control allows for significant improvement of laser material processing performance in a direct write system. The control system's performance is evaluated, and laser processing data on a variety of different materials is presented.

WAM1L-213 -- Implementation of a Silicon Driver for an Optically Controlled High Power Switching Application
Prashant Bhadri and Fred Beyette Jr, *University of Cincinnati*

The ever-increasing performance and economic requirements placed on commercial and military aircraft are resulting in the need for very complex avionic systems. To help alleviate some of the design complexity, fiber optic components have been suggested as an enabling technology that could allow the creation of an optical communications network routed throughout the avionic systems of an aircraft. The challenge has been the development of an optoelectronic switching technology that can withstand the high power and harsh environmental conditions common in a flight surface actuation system. Wide bandgap semiconductors such as Silicon Carbide offer the potential to overcome these operating conditions. Although SiC is not optically active at the near IR wavelengths where communications grade light sources are readily available, we have proposed a hybrid device that combines silicon based photoreceiver module with a SiC power transistor. We present in this paper the design and test results from a silicon driver chip that has recently been fabricated.

WAM1L-213 -- Characterization and Performance Evaluation of CMOS photodetectors implemented in Optoelectronic circuits
Prashant Bhadri and Prosenjit Mal, *University of Cincinnati,* Sunil Konanki, *IBM Corporation*, and Fred Beyette Jr, *University of Cincinnati*

The ability to produce a high performance monolithic CMOS photodetector could enable greater use of optics in short-distance communication systems and photonic information processing systems. The quest for a photodetector compatible with a high-volume high-yield CMOS process has yet to produce a clear winner, and has proven quite challenging. We present in this paper several different photodetector structures implemented with a conventional CMOS fabrication process that can be incorporated into optical data links and information processing systems. As a result, it combines the parallelism associated with optics and the data processing capabilities associated with CMOS logic.

WAM1L-214 -- Novel Circuits and Architectures

Wednesday: 9:00 am– 10:20 am

Chair: Michael Weeks

Georgia State University

WAM1L-214 -- ALU Design using Reconfigurable CMOS Logic

Ashok Srivastava and Chandra Srinivasan, *Louisiana State University*

Using the reconfigurable logic of multi-input floating gate CMOS, a 4-bit ALU has been designed in 1.5um technology for 3V operation. The ALU can perform four arithmetic and four logical operations. It is shown that this design uses significantly lesser number of transistors when compared to conventional designs.

WAM1L-214 -- A Hybrid Infinite/Finite Response (HIR) Filter

Michael Weeks and Baoan Wang, *Georgia State University*

Filters are used to implement signal transforms, and filter design is a very important part of the signal processing field. There are currently 2 types of filters available: the finite impulse response (FIR) filter, and the infinite impulse response (IIR) filter. While FIR filters have desirable traits such as stability (an absence of poles), IIR filters are able to generate outputs more efficiently. This paper combines the two types of filters by introducing a zero-counter, to make a hybrid impulse response (HIR) filter with desirable traits from both FIR and IIR.

WAM1L-214 -- A Simple and Fast Parallel Round-Robin Arbiter for High-Speed Switch Control and Scheduling

Si Qing Zheng and Mei Yang, *University of Texas-Dallas*, John Blanton, Prasad Golla, and Dominique Verchere, *Alcatel USA Research & Innovation*

A fast scheduling scheme is the key to the performance of a packet switch. Software approach is too slow for a high-speed switch. Many existing hardware solutions are based on round-robin arbiters. In this paper, we present a new round-robin arbiter design. We show that this arbiter is not only much faster than existing designs, it is also very much simpler. We believe this is the best design up to date.

WAM1L-214 -- A Novel Asynchronous Pipeline Architecture for CISC type Embedded Controller, A8051

Je-Hoon Lee, Won-Chul Lee, and Kyoung-Rok Cho, *Chungbuk National University*

In this paper, we propose an asynchronous processor A8051 is compatible with Intel 8051 which is a challenge of a pipelined asynchronous design for CISC type microcontroller. A8051 has special features such as an optimal instruction execution scheme that eliminates the bubble state, variable instruction length handling and multi-looping pipeline architecture for CISC machine. A8051 is composed of the 5 stages pipeline based on the CISC architecture. It is implemented with RTL level languages and a verified behavioral model is synthesized with 0.35micron CMOS standard cell library. as the result, A8051 shows about 18 times highter speed than that of Intel 80C51 and ablout 5 times higher than other asynchronous design 8051 in [1].

WAM1L-216 -- VLSI and Programming Logic Applications I
Wednesday: 9:00 am– 10:20 am
Chair: Jeffrey Coleman
Naval Research Laboratory

WAM1L-216 -- Comparison of Low-Power Multiplier Block Structures
Andrew Dempster, Suleyman Demirsoy, and Izzet Kale, *University of Westminster*

Multiplier blocks have been used primarily for the reduction of circuit complexity. Using new algorithms, it has been shown that they can also be used for effective reduction of power consumption in digital filter circuits. In this paper, the new GP score is used as a power measure to compare digital filter multiplier blocks designed using the BHM, RAGn and C1 algorithms.

WAM1L-216 -- Using Variable Length 13-ary, Radix-4 CSD Coefficients to Achieve Low-Area Implementations of FIR Filters
Linda DeBrunner, Victor DeBrunner, Deepak Bhogaraju and Venkata Naga, *University of Oklahoma*, and Jeffrey Coleman, *NRL*

Coefficient representations in the Canonical-Signed-Digit (CSD) number system are widely used because they lead directly to efficient addition/subtraction networks for implementation of weighted sums of 2's-complement input signals in filters. A recent radix-4 generalization of CSD can dramatically reduce network sizes. By combining radix-4 representations of coefficients with techniques for assigning different numbers of bits to different coefficients, we further reduce the area required for implementation.

WAM1L-216 -- Design of Linear-phase FIR Filters Combining Subexpression Sharing with MILP
Oscar Gustafsson and Lars Wanhammar, *Linkoping University*

In this work we formulate a mixed integer linear programming (MILP) problem for design of linear-phase FIR filters with low arithmetic complexity. By incorporating subexpression sharing in the problem formulation, the number of adders will be lower compared with previous approaches, where minimizing the number of non-zero bits of the coefficients has been the objective.

WAM1L-216 -- The application of 2-D logarithms to low-power hearing-aid processors
Roberto Muscedere and Jenifer Li, *University of Windsor*, Vassil Dimitrov and Graham Jullien, *University of Calgary*

This paper discusses the application of a new two-dimensional logarithmic number system (2DLNS) to the design of low-power processors for hearing-aid applications. The paper concentrates on the architecture of an optimized second base 8-band filterbank and an associated 16-bit binary to 2DLNS converter. The processor takes advantage of the low complexity, orthogonal nature, of the arithmetic used for multiplication and compression, and a simple binary converter. Details are provided for the filterbank and input converter, including the description of a 0.185m CMOS test chip recently submitted for fabrication.

WAM1L-218 -- Multiple Antenna Systems I
Wednesday: 9:00 am– 10:20 am
Chair: Robert Soni
Lucent Technologies

WAM1L-218 -- VFXLMS with a Weak Nonlinearity in the Secondary Path
Dayong Zhou and Victor DeBrunner, *The University of Oklahoma*

Recently, a modification of the Filtered-x LMS algorithm was presented that introduced the use of adaptive Volterra filters into the active control of nonlinear noise processes. Their Volterra Filtered-x LMS (VFXLMS) algorithm handles only a nonlinear main path. In this paper, we propose an extension of this method that can properly handle a weakly nonlinear secondary path (i.e., a nonlinearity in the actuators) as well as the nonlinear main path. We propose an algorithm that guarantees a stable and unbiased estimation with these nonlinear paths. The nonlinear adaptive FXLMS filter based on the Volterra series technique is developed, and a configuration is given based on the weak nonlinear secondary path. We provide some analytical results to motivate our method, and we provide simulations that indicate that our proposed algorithm performs well and is stable.

WAM1L-218 -- A Novel Algorithm For 2-D DOA Estimation in The Presence of Impulsive Noise
Ze-Jun Lu and Xian-Ci Xiao, *UESTC,* Heng-Ming Tai, *University of Tulsa*

This paper presents a particular array geometric configuration and the cross-covariation matrices for the subarray sensor outputs. Additionally, a new subspace-based two-dimensional (2-D) bearing estimation algorithm using fractional lower order statistics is proposed. This algorithm estimates the 2-D directions-of-arrival of array sensor signals in the presence of impulsive noise, and can be modeled as a complex symmetric alpha-stable (process. It exploits the infinite pth-moments for p > a and finite fractional pth-order moments for 1

WAM1L-218 -- A Bayesian Approach to Soft Parallel Interference Cancellation for Synchronous CDMA
Chris Schmitz and Ralf Koetter, *University of Ilinois at Urbana-Champaign,* and W. Jenkins, *Pennsylvania State University*

An attribute of the decorrelating detector is the ease in which the \emph{a posteriori} bit probabilities may be computed. In this paper, we use these \emph{a posteriori} bit probabilities (eg. $\pi_i\doteq \text{P}(b_i=+1\mid \underline{y})$) to replace the standard \emph{a priori} probabilities (eg. $\pi_i\doteq \text{P}(b_i=+1)\equiv\frac{1}{2}$) and find soft bit estimates that optimize particular cost functions under the Bayesian rule. The soft multiple access interference (MAI) bit estimates are suitable for a parallel interference canceller (PIC) and create a new genre of CDMA detection algorithms. The BER performance of this new genre is shown to better approximate that of the optimal MAP detector than previous methods.

WAM1L-218 -- Rank-1 Ambiguity DOA Estimation of Circular Array with Less Sensors
Wei Xaio and Xian-Ci Xiao, *UESTC,* and Heng-Ming Tai, *University of Tulsa*

Direction-Of-Arrival (DOA) of wide frequency band signals using large aperture array might meet ambiguity problem. The array is said to be of rank-1 ambiguity for DOA estimation if any two steering vectors of the array manifold are linearly dependent. The Uniform Circular Array (UCA) is an important planar array for its almost invariant direction pattern and all azimuth coverage. In general, the UCA is considered to be free of (rank-1) ambiguity in DOA estimation. However, it might not be the case for the UCA with fewer sensors. In this paper, we show that the UCAs with sensors (M) less than or equal to six are of rank-1 ambiguity (except M = 5). In addition, we propose an approach to construct a rank-1 ambiguity free non-uniform circular array (NUCA) with six sensors. We demonstrate that a NUCA with six sensors designed by this approach is rank-1 ambiguity free in

a wide frequency band with the ratio of circular array radio to the wavelength ranging from 0.5 to 3. Computer simulation and the field test are shown for the validation purpose.

WAM1L-219 -- Neuro Control
Wednesday: 9:00 am– 10:20 am
Chair: Mohammad Menhaj
Oklahoma State University

WAM1L-219 -- A Neuro-controller with Guaranteed Stability
Mohammad Menhaj, *Oklahoma State University*

This paper introduces a novel neuro-adaptive control. The new learning algorithm guarantees the stability of a class of closed loop neural network control systems. The underlying control system represents a special class of non-linear systems. The neuro-controller, which indeed represents a direct adaptive controller, guarantees the closed loop stability for any arbitrary initial values of states, neural network parameters and any unknown-but-bounded disturbances, provided that some soft conditions are satisfied. No additional controllers or robustifying terms are needed. Neural network weight matrices are adapted online with no initial offline training.

WAM1L-219 -- Smoothing the Control Action for NARMA-L2 Controllers
Arjpolson Pukrittayakamee, Orlando De Jesus, and Martin Hagan, *Oklahoma State University*

There have been many approaches to the use of neural networks in control systems, such as the NARMA-L2 Controller, introduced by Narendra and Mukhopadhyay. One disadvantage of this controller is that it often produces chattering in the control action. In this paper we investigate the addition of linear feedback to the NARMA-L2 controller in order to smooth the control action. We show that under certain circumstances this linear feedback can cause problems of stability and increased steady state errors, especially when the plant model is inaccurate. These problems can be reduced significantly by the use of appropriate design strategies, which are presented in the paper.

WAM1L-219 -- The OSU Multi-Vehicle Coordination Testbed
Rafael Fierro and EzzAldeen Edwan, *Oklahoma State University*

In this paper we present the OSU Multi-Vehicle Coordination Testbed, a group of nonholonomic robots for testing and implementing hybrid control approaches for formation control, multi-agent coordination, multi-robot learning, and real-time wireless networked control system design. The vehicles are equipped with a suite of sensors, a vision system and wireless Ethernet for communications. The testbed will allow us to carry out experimental research to verify theoretical results that have been validated using only simulation. In addition, we describe a framework for adaptive leader-following formation control. The novel aspect of this research is that we explicitly consider the dynamics of the vehicles and develop a modular adaptive formation control scheme.

WAM1L-219 -- Autonomous Robot Navigation System Using a Novel Value Encoded Genetic Algorithm
Thomas Geisler and Theodore Manikas, *University of Tulsa*

This paper describes the development of a genetic algorithm (GA) based path-planning software for local obstacle avoidance. The GA uses a novel encoding technique, which was developed to optimize the information content of the GA structure. Simulation results were used to further optimize the developed software and determine its optimum field of operation. The results show that the GA finds valid solutions to the path-planning problem within reasonable time and can therefore be used for real world applications.

WAM1L-221 -- Adaptive Signal and Image Processing I

Wednesday: 9:00 am– 10:20 am

Chair: Guoliang Fan

Oklahoma State University

WAM1L-221 -- Output Distribution of Fuzzy Weighted Median Filters

Yao Nie and Kenneth E. Barner, *University of Delaware*

Fuzzy weighted median (FWM) filters are developed by utilizing concepts of fuzzy ordering in weighted median (WM) filters framework and have great advantages over their crisp counterparts. In this paper, two important properties of fuzzy ordering --- element invariant property and order invariant property --- are investigated, which shall serve as the theoretical justification of FWM filters. Based on these two properties, we derive the analytical expressions for the output distribution of FWM filters, which provide systematic methods to study the statistical properties of FWM filters.

WAM1L-221 -- On the Teager-Kaiser Energy Operator "Low Frequency Error"

Matthew Lipsey and Joebob Havlicek, *University of Oklahoma*

We investigate frequency-dependent frequency estimation errors in the DESA-2 energy separation algorithm associated with the discrete Teager-Kaiser energy operator (TKEO). The TKEO and DESA-2 algorithm associate instantaneous amplitude and frequency functions to a real-valued discrete-time signal. It has been observed informally that there seems to be a frequency dependent error in the instantaneous frequency estimates delivered by the approach, where the error is more pronounced at lower frequencies. By studying quadratic phase signals, we demonstrate that this TKEO ``low frequency" error does in fact exist and is related to both the magnitude frequency and the signal chirp rate.

WAM1L-221 -- A New Technique for Motion Estimation of Water Borne Micro-organisms in the Hartley Domain

Devendra Bajpai and Manohar Das, *Oakland University*

This paper proposes a technique for estimating motion of water borne micro-organisms using the Discrete Hartley Transform (DHT). The Hartley Transform has properties similar to those of the Fourier Transforms, but has speed and memory advantages over the Fourier, discrete cosine transform (DCT) or discrte sine transform (DST) based methods. First denoising is carried out using a soft threshold and a method similar to wavelet denoising. Next, motion detection is carried out using a two-stage temporal change detection technique. Also, a block matching technique in the Hartley domain is proposed, which can detect micro-organism motion by using the phase shift property of the DHT. Position estimation of multiple objects can be performed using this technique.

WAM1L-221 -- A 2-D Filtering Structure with Neural Networks for Gaussian Noise Cancellation and Edge Preservation in Images

Justo Seiji Oshino-Ortiz and Masayuki Kawamata, *Tohoku University*

In this paper, we propose a structure of a two-dimensional adaptive digital filter for cancellation of white Gaussian noise in images and edge preservation. This structure is composed by three parts. We use a two-dimensional filtering algorithm to avoid disturbance due to one-dimensional filtering, a neural network to update the filter coefficients, and a variable-size filtering window to preserve edges. Experimental results show that a filter with the proposed two-dimensional structure cancels the white Gaussian noise and preserves the edges of the image better than those filters based on a one-dimensional filtering algorithm or one that does not consider the edges.

WAM1L-223 -- Speech Processing and Analysis
Wednesday: 9:00 am– 10:20 am
Chair: Mary Kohler
Department of Defense

WAM1L-223 -- Improving Analysis Techniques for Automatic Speech Recognition
Douglas Oshaughnessy, *INRS-Telcommunications*

Automatic speech recognition is now feasible even in speaker-independent applications over the telephone. However, recognition is reduced in noisy or mismatched conditions. Traditional approaches with cepstral analysis and filterbanks will be reviewed. Simpler spectral analysis methods are proposed, which focus on the locations of spectral peaks. Such techniques have similarities to traditional formant tracking, but do not suffer from the need to estimate formant peaks for all time frames. Advantages in terms of robustness against channel noise as well as mismatched train-and-test conditions will be noted. The utility of better exploiting knowledge of human speech communication will be emphasized.

WAM1L-223 -- Language Identification Using Shifted Delta Cepstra
Mary Kohler and Michael Kennedy, *U.S. D.o.D.*

A variety of speech identification technologies currently use Gaussian mixture models. Until recently, however, they were considered inferior to parallel phone recognition language modeling for identifying the language of a speaker. Experiments in the last year have shown that Gaussian mixture models can provide high performance language identification when shifted delta cepstra are used as the feature set. Not only can they achieve comparative or even superior performance to parallel phone recognition language modeling, Gaussian mixture models also require less computation. Performance can be further improved by altering the shifted delta cepstra parameters and the number of mixtures. The optimal parameter set varies depending on the languages to be identified. This paper describes a method for finding the optimal parameters for identifying a set of languages, specifies these parameters for some typical language identification tasks, and provides a performance comparison.

WAM1L-223 -- Internet-Accessible Speech Recognition Technology
Kaihua Huang and Joe Picone, *Mississippi State University*

Speech recognition systems can be viewed as an application of complex pattern recognition and machine learning algorithms. The developmen tof such a state of the art system is a time-consuming and infrastructure-intensive task. The Institute for Signal and Information Processing (ISIP) developed one of the first fully-functional public domain speech recognition system. In this paper, we introduce the major components of this system, which include a digital signal processing front-end which generates feature vectors from the speech signal; a Hidden Markov Model (HMM) trainer which estimates acoustic model parameters; a hierarchical search decoder which implements an efficient time-synchronous Viterbi beam search.

WAM1L-223 -- Sensitivity of MIL-STD-3005 MELP to Packet Loss on IP Networks
Edward Daniel and Keith Teague, *Oklahoma State University*

The sensitivity of military standard MELP (MIL-STD-3005) to randomly deleted frames on an IP network is studied. Frame deletion occurs when packets are lost or arrive too late to be useful in a voice-over-IP (VoIP) application. Network errors including packet loss, burst loss, jitter and out-of-order packets are simulated. The quality of reconstructed speech is measured by spectral distortion and informal listening tests.

WAM1L-225 -- MPLS, MPLambdaS, and GMPLS Networks I

Wednesday: 9:00 am– 10:20 am

Chair: Harleen Chhabra

ExxonMobil

WAM1L-225 -- Analysis of Nonpreemptive Priority Queueing of MPLS Networks with Bulk Arrivals

Hooi Miin Soo and Jong-Moon Chung, *Oklahoma State University*

In this paper, the queueing performance of multiprotocol label switching (MPLS) systems is analyzed through the nonpreemptive M/M/m/K finite queueing model with bulk arrivals, where the traffic burstiness characteristic is considered. The analytical results reveal the queueing time relation of different priority classes of data traffic due to the MPLS classification, queueing, and scheduling (CQS) operations, which provide design guidelines for future label switching routers (LSRs). This can provide an analysis of MPLS routers and network streams for various system server topologies applying the nonpreemptive priority M/M/m/K queueing model in order to assist network system designers in the hardware/firmware development.

WAM1L-225 -- A Novel Analysis of Queue Length in Differentiated Services Networks, with Self-Similar Arrival Processes

Zhi Quan and Jong-Moon Chung, *Oklahoma State University*

It is well known that traditional analytic methods of queueing systems are based on the distributions of inter-arrival time and service time. However, it is quite inconvenient to employ these methods directly to the analysis of current self-similar (SS) traffic models. In this paper, we first derive a novel analytic model based on arrival rate and service rate for single-class steady-state queueing systems. In addition, the derivations are extended to provide upper and lower boundary conditions for multi-priority queues in networks deploying differentiated services (DS). This analytical model has also been shown to be directly applied to the analysis of DS effects on SS traffic. The results illustrate the possible performance gain in queue length of the priority classes that DS can provide compared to a network that does not deploy DS.

WAM1L-225 -- Mobility: A VPN Perspective

Ravi Bhagavathula and Ravi Pendse, *Wichita State University*

Mobile Computing is becoming increasingly important due to the rise in the number of portable computers and the desire to have continuous network connectivity to the Internet irrespective of the physical location of the node. Mobile IP, the more popular global mobility solution, was designed to support mobility of a single host. Even though the same protocol can be applied in the case of network mobility, providing connectivity to mobile networks introduces many issues related to the scalability, security and QoS. Instead, a mobile network can be cited as a remote site, trying to establish secured communication with the home network. This view of mobile network solves many issues related to QoS, security and scalability. The objective of this paper is to explore the possibility of using different VPN techniques to provide connectivity for mobile network and measure the corresponding end-to-end performance of real time traffic and best effort traffic patterns.

WAM1L-225 -- MPLS Multicasting Through Enhanced LDP and RSVP-TE Control

Jong-Moon Chung, Mauricio Subieta Benito, Grace Cho, and Pravin Rasiah, *Oklahoma State University*, and Harleen Chhabra, *EXXON Mobile*

This paper addresses the required extensions to the MultiProtocol Label Switching (MPLS) signaling protocols, Resource Reservation Protocol with Traffic Engineering extensions (RSVP-TE) and Label Distribution Protocol (LDP), to support MPLS network multicasting functionalities. These extensions to the signaling protocols will enable MPLS networking to conduct all required multicasting features that IP multicasting protocols are capable of, while adding on the feature benefits of MPLS traffic engineering.

WAM1P-140 -- Communications Systems
Wednesday: 9:00 am– 10:20 am
Chair: Edward Daniel
Oklahoma State University

WAM1P-140 -- Wireless Internetworking Protocol (WIP)

Kannan Srinivasan and Jong-Moon Chung, *Oklahoma State University*

In this paper, a novel IP layer protocol is introduced under the name of wireless internetworking protocol (WIP). WIP was designed to provide reliable and steady continuous data transfer flow in the Internet protocol (IP) layer over wireless communications systems. WIP technology enables the wireless hosts to be mobile while establishing soft handoffs in support of high quality of service (QoS) for real-time data traffic over mobile wireless environments. WIP technology solves some of the fundamental problems of mobile IP (MIP) and route optimized MIP (ROMIP), such as the triangle routing problem and the requirement of redundant buffering, comparing and transferring of stacks of data between the foreign agents and the mobile host (MH). Unlike in Mobile IP and ROMIP, where only smooth handoff procedures are possible in which the packets during handoff are buffered and then delivered after the handoff is complete, WIP enables make-before-brake soft handoff procedures, which enables end-to-end reliability through transport control protocol (TCP) connections to provide full connectivity during handoff procœdures thereby reducing the number of undetectable lost packets during the handoff instants.

WAM1P-140 -- Future NarrowBand Digital Terminal

Edward Daniel, Keith Teague, William Beck, Robert Sleezer, Joe Hershberger, Jerry Brewer, and Josh Raymond, *Oklahoma State University*

The Future NarrowBand Digital Terminal (FNBDT) is a new signaling plan being developed by the government supporting secure multimedia communications. FNBDT provides a network independent architecture for communications over concatenations of wired and wireless networks. The development of an FNBDT application supporting secure voice communication using the MIL-STD-3005 MELP and Rijndael based counter mode encryption is described.

WAM1P-140 -- Capacity Analysis of Macroscopic Diversity Reception Combining Spread Spectrum Channels in Mobile Communication Environments

Jong-Moon Chung, Lijy Jose Kallidukil, and Moses Lynn George, *Oklahoma State University*

This paper investigates the channel capacity of direct sequence spread spectrum (DSSS) code division multiple access (CDMA) wireless mobile communication systems in Rayleigh distributed lognormal shadowed fading channels. The proposed model builds upon the former Jakes model [Jakes1974] of macroscopic diversity for achieving enhanced data rates at lower bit error probabilities in shadowing environments. Analytical results and computer simulations are provided to substantiate the findings. The paper also discuss the implementation and benefits of applying this model as a possible 4th Generation high-speed broadband wireless mobile communication topology.

WAM1P-140 -- An Vertical Layered Space-Time Coding and the Symbol Detection

Zheng Zhao, *Jiaotong University*

Recent results in information theory have demonstrated the enormous potential of wireless communication systems with antenna arrays at both the transmitter and receiver. To exploit this potential, Vertical layered space¨Ctime codes is attractive for its relative simplicity and robust high-capacity. Thus far, vertical layered space¨Ctime code assumed that perfect estimates of current channel fading conditions are available at the receiver. In certain situations, however, it may be difficult or costly to estimate the channel accurately. In this paper, by applying the subspace method, we propose a vertical layered space-time code to detect symbols

without the knowledge of the channel. From Monte Carlo simulations, we show that performance can approach the detection method needed the knowledge of the channel.

WAM1P-140 -- Interoperability Enhancement Recommendations for MPLS and ATM PNNI Networks

Jong-Moon Chung, Rajpamal Pethuraj, and Akhil Pandya, *Oklahoma State University*

This paper focuses on providing technical solutions to the multiprotocol label switching (MPLS) networking label distribution protocol (LDP) when interoperating with the asynchronous transfer mode (ATM) private network-to-network interface (PNNI) and compares this with the interoperating procedures of the user network interface (UNI) topology.

WAM1P-140 -- Multiple LSP Routing Network Security for MPLS Networking

Jong-Moon Chung, Sunitha Panguluru and Dongfang Liu, *Oklaloma State University*, and Raymond Garcia, *Georgia Institute of Technology*

In this paper, network security algorithms and control protocol enhancements for multiple LSP routing in MPLS networks are investigated. Most of the former research on multiple-path routing has been focused on using multiple paths as a topology to improve the throughput and the robustness of data transportation over packet switching networks. The developed topology absorbs these benefits and extends the features to include extreme levels of WAN security. The results show that the proposed topology provides extreme levels of protection against path information sniffing and deciphering. In addition, the proposed topology has numerous useful applications in wireless networking.

WAM1P-140 -- Maintaining Chaotic Synchronization in a Variable Time Delay Channel and Its Application in Computer Communication Security

Abdelatif Elkouny and Nabil Zakaria, *University of Kent*

This paper focuses on how to synchronize two chaotic systems, when they are connected, using a variable time delay channel. Applying the proposed technique for secure communication, an encryption algorithm that can be used for text messages, images and recorded voice with high security, is also presented. The simulation results reveal that signals to chaos ratio of -246dB and synchronization have been achieved.

WAM1P-140 -- A Reconfigurable Analog-To-Digital Converter For UTRA-TDD Mobile Terminal Receiver

Aleksandar Stojcevski, Jugdutt Singh, and Aladin Zayegh, *Victoria University*

A reconfigurable analog-to-digital converter (ADC) has been proposed for a mobile terminal. This architecture scales the digital word length (bits) by automatically monitoring desired power and adjacent channel interference power. This leads to power consumption savings, depending on the number of bits used. The architecture can scale between a minimum of 4 bits and maximum of 16 bits. The new reconfigurable ADC was applied to Time-Division-Duplex (TDD) mode of UMTS Terrestrial Radio Access (UTRA) system and results show that this reconfigurable ADC can save up 75 % of the power consumption when compared with the power consumption of a standard 16-bit analog-to-digital converter.

WAM1P-140 -- Virtual Laboratory Development for Persons with Vision Disabilities

Jong-Moon Chung, Krishnaveni Ramasamy, Zia Mulla, Vizayakumar Kotikalapudi, Girirajan Thiyagarajan, Mark Weiser, George Scheets, and Ramesh Sharda, *Oklahoma State University*

The Virtual Laboratory (VLab) is focused on providing same-time different-place group-interactions, allowing full real-time virtual-interaction of voice/video/data information of the Internet,systems, equipment, and facilities for vision disabled persons. The VLab interactive-monitor uses piezoelectric technology for graphical display and includes a novel Braille Markup Language (BML) interface with HTML and WAP.The BML interfaces

enables conversion of all types of existing web sites and facility/equipment control information to be displayed on the VLab interactive Braille monitor.

WAM1P-140 -- A Reduced Complexity Low Voltage 1-Bit High-Order Digital Delta-Sigma Modulator for Fractional-N Frequency Synthesis

Rasoul Dehghani and Seyed Mojtaba Atarodi, *Sharif University of Technology,* Babak Bornoosh and Ali Afzali Kusha, *University of Tehran*

In this paper, a reduced complexity third-order digital delta-sigma modulator for fractional-N frequency synthesis is presented. The modulator consists of two sub-blocks and has a single bit output which makes it best for this application. A good shaping of quantization noise is achieved using a new architecture for a digital third-order delta-sigma modulator. The hardware required for this modulator is considerably less compared to previous works. The FPGA implementation of the whole system shows an SNR of 94dB and a dynamic range of 0.65 with an oversampling ratio of 167. The post-layout simulation of the digital circuit using 0.25mm CMOS technology predicts a maximum operating frequency of over 60MHz at a supply voltage of 1.5V.

WAM2L-209 -- Analog Filters II

Wednesday: 10:40 am– 12:00 pm

Chair: Jin Liu

University of Texas at Dallas

WAM2L-209 -- A 100MHz 7th-order gm-C filter with a wide-range transconductance amplifier

Joongho Choi, and Sunki Min, *University of Seoul*

This paper describes the gm-C filter design with the proposed wide-range transconductance amplifier. The transconductance amplifier includes the auxiliary positive feedback differential pair to enhance the operating range with small variation of gm value. The 100MHz 7th-order 0.05o equiripple linear-phase lowpass filter is designed in a 0.35-mm CMOS technology. The 3-dB frequency can be finely programmed and maintained through on-chip tuning PLL. The filter operates at the single power supply voltage of 3.3V.

WAM2L-209 -- A 2.5-V, 0.35 ìm CMOS transconductance-capacitor filter with enhanced linearity

Alexander Korotkov and Dmitry Morozov, *St.Petersburg State Technical University*, Hans Hauer, *Fraunhofer Institute for Integrated Circuits, Erlangen*, and Rolf Unbehauen, *University Erlangen-Nurenberg*

A CMOS transconductance-capacitor (Gm-C) filter with enhanced linearity for low-voltage applications is presented. The proposed design is based on a transconductance amplifier with enhanced linearity. For the elimination of the amplifier harmonic level the compensation principle is used. The transconductor consists of two amplifiers connected in parallel. The input transistors of the first transconductor are working in the saturation region, while the input transistors of the other one are in the triode region. The device was realized as a balanced fifth-order 1MHz low-pass Bessel filter in 0.35ìm CMOS technology. The filter operates with a low supply voltage of +2.5 Volt. A comparison shows that the discussed filter provides a higher linearity (from 3 to 8 dB) than known circuits with the exception of the filter based on a degenerated transconductor. But it is noted that there are some difficulties to use the last approach for low-voltage application.

WAM2L-209 -- Compact Sub-Hertz OTA-C Filter Design with MOS Interface-Trap Charge Pump

Adriana Becker-Gomez, Ugur Cilingiroglu, and Jose Silva-Martinez, *Texas A&M University*

Very compact tunable sub-hertz OTA-C filters are designed with MOSFET interface-trap charge-pumping transconductors, and fabricated in 0.5mu CMOS. The lowpass filter is built with 15pF integration capacitor, occupies 0.0346 square millimeter and is tunable down to 0.18Hz. The bandpass contains four 15pF capacitors, occupies 0.188 square millimeter, and is tunable in the range 0.3Hz-100Hz.

WAM2L-209 -- Linearized OTAs for High-frequency Continuous-time Filters: A Comparative Study

Mingdeng Chen, Ahmed Mohieldin, and Jose Silva-Martinez, *Texas A&M University*

This paper presents a comparative study of three single-stage high frequency linearized OTAs for the design of high-performance continuous-time filters. The advantages and disadvantages of each structure are discussed. The two pseudo-differential OTAs are suitable for very low-voltage applications. One OTA is suitable for very high frequency applications and the other one has a very large linear signal swing and a large transconductance tuning range. The third OTA is based on complementary differential pairs and has very low power consumption. Design examples and experimental results are presented to demonstrate the performance characteristics of each structure.

WAM2L-211 -- Passive RF and Microwave Systems
Wednesday: 10:40 am– 12:00 pm
Chair: James West
Oklahoma State University

WAM2L-211 -- Design of RF Integrated Inductors by Geometric Scaling
Nader Badr, and Robert Weber, *Iowa State University*

This paper presents research related to the design and characterization of geometrically scaled monolithic RF inductors. The geometries of on chip passive RF components are scaled up by a factor 'a'. The scaled model is characterized at a scaled down frequency range by a factor '1/a'. The scattering parameters extracted from the scaled model reflect the behavior of the original on-chip model at the original frequency range. Two port scattering parameter measurement results of the scaled model show agreement with the simulated original model using an Electromagnetic (EM) simulator with good accuracy.

WAM2L-211 -- Multi-Port Network Modeling of Multi-Layer Planar Circuits Containing Ground Plane Slots
Amirreza Khajehnasiri and Safieddin Safavi-Naeini, *University of Waterloo*

A new approach for Multi-Port Network Modeling (MNM) of multi-layer planar circuits containing slots is introduced. Generalized network formulation for aperture problems is combined with Okoshi's model for planar circuits to obtain a unified circuit model for two planar circuits coupled through a slot of arbitrary shape in their common ground plane. The methodology, which can be easily generalized to structures having more than two layers, is clarified by applying the method to a multi-layer microstrip filter.

WAM2L-211 -- Technology Migration Effects on Signal Integrity of Single On-Chip Interconnect
Hani Ghali, *Ain Shams University*

A full-wave electromagnetic EM solver has been used to investigate the effects of technology migration on signal integrity parameters for a single on-chip interconnects. In addition, the effects of using new interconnect materials and/or low-k dielectrics have also been investigated. The EM solver has been used to calculate the electromagnetic quantities S parameters for the single on-chip interconnect, which are then transformed to an RLCG transmission-line equivalent circuit model. Consequently, a SPICE-like simulator is used to evaluate the signal integrity parameters.

WAM2L-211 -- Compact Low-Pass Filter using a Slow-Wave Structure
Carlos Saavedra, *Queen's University*

In this paper a compact low-pass filter that makes use of coupled microstrip lines is investigated. A slow-wave structure is used to equalize the even and odd mode phase velocities of a pair of coupled microstrip lines and thereby improve the directivity of the coupled lines. Two low-pass filters were fabricated: one using the slow-wave structure and one using conventional coupled lines. The results reveal that the rejection of the low-pass filter is significantly improved by using the slow-wave structure.

WAM2L-213 -- Optical Circuits and Systems II

Wednesday: 10:40 am– 12:00 pm

Chair: Sherif Michael

Naval Postgraduate School

WAM2L-213 -- Designing Transimpedance Amplifier and Limiting Amplifier for 10 Gb/s Optical Communications

Mohammad Reza Samadi Boroujeni, Aydin Karsilayan, and Jose Silva-Martinez, *Texas A&M University*

Transimpedance amplifier (TIA) and Limiting amplifier (LA) are two of the most important circuits in optical communications. SiGe-based low noise differential TIAs with transimpedance gain of 63dB for 10Gb/s link are introduced. To amplify signal after TIA, we designed a novel LA. The LA gives a differential output with 0.6 VPP. Proper biasing and feed forward paths decrease power in TIA+LA to 60mW.

WAM2L-213 -- A 5-Gbit/s CMOS Optical Receiver Frontend

Francis Beaudoin and Mourad El-Gamal, *McGill University*

An optical receiver frontend achieving a 5-Gb/s bit-rate was realized in a 0.18um CMOS process. The preamplifier has a measured gain of 58.7dBOhm, an input-referred current noise of 13pA/rt Hz, and uses a constant-k filter to extend the bandwidth. The TIA is followed by a chain of amplification stages with passive offset control. The receiver operates from a 1.8V power supply, while dissipating only 47mW (97mW with the complete test circuitry and buffers). The circuit is housed in a standard CFP24 package.

WAM2L-213 -- Development of an FPGA for Multi-Technology Applications

Prosenjit Mal and Fred Beyette, *University of Cincinnati*

We present here a novel architecture for a Field Programmable Gate Array that incorporates multi-technology blocks to work in multi-technology environments (ex. combinations of Digital Logic, CMOS based Analog, Photonic, MEMS, Microwave, etc.). Based on a modular approach that resembles conventional FPGA design, the architecture presented here is robust and scalable. Implemented using a conventional CMOS VLSI device technology, this new FPGA architecture will enable the design of reconfigurable systems the incorporate technologies outside of the traditional electronic domain

WAM2L-213 -- Fabrication of Cantilevered Near-Field Probe Arrays Using MEMS Technology

Pradeep Srinivasan, Fred Beyette, and Ian Papautsky, *University of Cincinnati*

This paper describes fabrication of cantilevered near-field probe arrays using MEMS technologies on glass wafers, which can be coupled to on-chip detector arrays. The probe arrays are formed by dicing of glass wafers, followed by a two-step etch process. Arrays of up to 10 2-cm long probes at 450 um center-to-center spacing and approximately 800 nm tips have been demonstrated. The measured loss coefficients vary from 10 to 1 dB/cm depending on etch duration. The presented process enables fabrication of large arrays of variable center-to-center spacing, promising to simplify integration with CMOS photoreceivers arrays for future high-density data storage/retrieval.

WAM2L-214 -- Third and Fourth Generation Wireless Systems
Wednesday: 10:40 am– 12:00 pm
Chair: Annamalai Annamalai
Virginia Tech

WAM2L-214 -- A New Efficient Dynamic-Iterative Technique for Turbo Decoders
Ibrahim Al-Mohandes and Mohamed Elmasry, *University of Waterloo*

Turbo coding has been adopted by the International Telecommunication Union as a channel coding standard for third-generation wireless high-speed data services. Turbo decoders consume a large amount of energy due to the iterative decoding feature. This paper presents a new dynamic-iterative technique that reduces the number of iterations in a turbo decoder at both improved and distorted channel conditions. Simulations show that the proposed technique reduces the number of decoding iterations by about 40% compared to the static-iterative case, over a signal-to-noise ratio range of -1 to 2 dB. It is also shown that the iteration reduction given by the new method is superior to those of the other low-complexity dynamic-iterative methods, with a decoding performance close to the best of these methods.

WAM2L-214 -- Systolic Equalizer Structures
Thomas Sexton and Jari A. Parviainen, *Nokia Mobile Phones*

Algorithms for the detection of an 8-PSK signal distorted by passage through a cellular radio channel are reviewed. The goal is to provide performance and vlsi implementation comparisons. The main contribution of this paper is the presentation of a systolic equalizer for Viterbi equalization of an 8-PSK signal. Variations of the systolic linear array are also discussed.

WAM2L-214 -- A new Pi-Model of Bipolar Transistor Noise for Circuit Analysis and Simulation & Technique to Reduce Phase Noise in Bipolar Oscillators
Leonard Forbes, Iswahyudi Chandra, and Chengwei Zhang, *Oregon State University*

A new bipolar transistor noise model for SPICE and SPICE based simulation software is introduced. The parameters of the new bipolar transistor noise model are predicted using MATLAB and the results are compared with measurement results. The new model avoids the unreal situation in the current model where the transistors will have no l/f noise in the collector current output if the impedance in the base circuit is small. Low frequency feedback is utilized to reduce the effect of base-emitter current 1/f noise in bipolar transistor oscillators. A resistance in the emitter that is bypassed at the higher oscillation frequency but not at the lower 1/f noise frequency will reduce the nonlinear mixing of the two current signals and phase noise in oscillator. The concepts are demonstrated by a simple low frequency oscillator.

WAM2L-214 -- Comparison of Initial Cell Search Algorithms for 3GPP W-CDMA Systems Using Cyclic and Comma Free Codes
Sanat Kamal Bahl, Jim Plusquellic, and Joseph Thomas, *University of Maryland Baltimore County*

This paper describes a new cell search design (CSD) to achieve faster synchronization between the mobile station and the base station. The Improved CSD which uses Cyclic Codes is compared to the 3GPP CSD which uses Comma Free Codes in terms of a) hardware specifications on a Xilinx Virtex-E FPGA and b) acquisition time measures for different probabilities of false alarm rates. Our results indicate that for a AWGN channel model in a high signal-to-noise ratio environment the Improved CSD has a faster acquisition time and lower gate count under the same constraints for both the designs.

WAM2L-216 -- VLSI and Programming Logic Applications II

Wednesday: 10:40 am– 12:00 pm

Chair: Jeffrey Coleman

Naval Research Laboratory

WAM2L-216 -- FPGA System-on-Chip Soft IP Design: a Reconfigurable DSP

Maurizio Martina and Fabrizio Vacca, *Politecnico di Torino*

In this paper an architecture for a scalable DSP core is proposed. Due to the increase of system resources available on FPGA, the System-on-Chip paradigm can be borrowed from classical silicon implementations into reconfigurable environments. Despite the increasing importance gathered by reconfigurable computing, a lack of retargettable soft-processor IP is felt. This IP aims to fill the existing gap between specific coprocessor units and general purpose soft cores. The proposed architecture exhibits interesting figures both in terms of area occupation and maximum operative clock frequency. Good experimental results have been obtained running at 89 MHz on a XILINX XCV1000.

WAM2L-216 -- Comparison of Various Numerically Controlled Oscillators

Sameer Kadam, Dhinesh Sasidaran, Amjad Awawdeh, Louis Johnson, and Michael Soderstrand, *Oklahoma State University*

The focus of this paper is to present a comparison of three types of digital sinusoidal oscillators. The first system is a look-up table based numerically controlled oscillator (NCO), the second is a direct form digital oscillator and the third is a system employing the COordinate Rotational DIgital Computer (CORDIC) algorithm. The three systems were implemented on a Virtex 800 Series FPGA.

WAM2L-216 -- Rapidly Configurable Coarse-Grained FPGA Architecture for Digital Filtering Applications

Shu-Shin Chin, Wei Wu, and Sangjin Hong, *SUNY at Stony Brook*

This paper presents a rapid reconfigurable coarse-grained FPGA architecture targeted for FIR filter, LMS adaptive FIR filters with multiple correlation and FFT/IFFT for digital filtering applications. The proposed architecture can configure up to four pipelined radix-4 or radix-2 2048 point FFT/IFFT, two 32-tap LMS filters or two 64-tap multiple FIR filters. By reducing unnecessary switching and using general purpose routing resources, used extensively in fine-grained FPGAs, our approach can achieve the flexibility of a fine-grained FPGA with the performance and area efficiency similar to that of an ASIC.

WAM2L-216 -- Hardware efficient Octaphase-shift keying detector

Shyam Sunder Uma Chander, Amjad Awawadeh, Andoche Kichenaradjou, and Michael Soderstrand, *Oklahoma State University*

A very simple LMS-based adaptive notch filter implemented in FPGA's can be used for carrier recovery of an Octaphase shift-keying signal. The key aspect of our paper lies in the alternative approach in the realization of carrier frequency detection or synchronization circuit. The carrier frequency after detection is used in the conventional Octaphase shift-keying detector. Also the demodulator has a simple hardware realization that does not require a reference signal.

WAM2L-218 -- Multiple Antenna Systems II
Wednesday: 10:40 am– 12:00 pm
Chair: Robert Soni
Lucent Technologies

WAM2L-218 -- Link Adaptation and Channel Prediction in OFDM Communication Systems

Robert Heath, *University of Texas at Austin,* and Antonio Forenza, *ArrayComm Inc.*

The goal of link adaptation is to use the power and the spectrum more efficiently to enhance throughput and system capacity. Typical link adaptation schemes use an estimate of link quality to choose the highest rate modulation and FEC coding scheme that guarantees a predefined target PER. In OFDM systems the channel statistics are collected in both time and frequency domain and the link quality region is defined through some estimation functions. Link adaptation is challenging in OFDM systems since, due to bandwitdth limitations, it is often not possible to convey the full channel state to the transmitter and thus per-tone bit loading is infeasible. In this paper we present an adaptive modulation technique for OFDM communication systems. For the link adaptation to achieve the optimal performance, perfect channel state information (CSI) is required. In case of high Doppler, however, it is hard to feedback the CSI with reasonable delay, compared to the channel coherence time. Therefore, prediction of the future channel behavior is required. We present an algorithm to predict the evolution in time of each OFDM tone. We then propose an equivalent and more efficient way to apply the linear prediction to the channel taps, in an OFDM system. Finally, we show an adaptive prediction algorithm, which optimizes the prediction parameters to the changing Doppler conditions.

WAM2L-218 -- Channel Equalization Using Adaptive Subband Filters

Geoff Williamson, *Illinois Institute of Technology,* and Daniel Bailey, *Northrup Grumman Corporation*

A novel channel equalization scheme based on adaptive subband filtering is described and analyzed. The structure integrates simultaneous transmission of training and data sequences over separate subbands. The use of crossband filters in a subband equalizer is shown to enable exact reconstruction of an equivalent fullband equalizer, thereby avoiding delay and aliasing. Structural relationships between the subbands are derived that demonstrate the need to use only a single subband error signal to adjust the entire fullband equalizer. Adaptation based only on the training subband thus permit equalization of the data subbands. Performance benefits and the relationship to OFDM schemes are discussed.

WAM2L-218 -- Series-Cascade Nonlinear Adaptive Filters

Vikram Hegde and William Jenkins, *Penn State University*

A memoryless nonlinear system can be often described by a power series expansion such as the Taylor series. Nonlinear systems with memory can be represented by the well known Volterra series, which is really a generalization of the Taylor series that incorporates memory into the representation. Furthermore, specific classes of nonlinear systems can be represented by one of three models: i) the Wiener model (cascade of a linear filter followed by a memoryless nonlinearity), ii) the Hammerstein model (cascade of a memoryless nonlinearity followed by a linear filter), or iii) a hybrid combination of the Wiener and Hammerstein models known as the LNL model (series-cascade of a linear filter, a memoryless nonlinearity, and a second linear filter. In this paper, we first consider LNL adaptive systems with an FIR linear system at the input stage and a FIR or an IIR linear system at the output stage. We then consider combining the linear input stage and the memoryless nonlinear stage of the LNL model, resulting in the series-cascade of a Wiener system with a linear output stage.

WAM2L-218 -- Symbol Detection Based on Subspace Method for Diversity System

Zheng Zhao, *Jiaotong University*

Delay diversity is an effective transmit diversity technique to combat adverse effects of fading. Thus far, previous work in delay diversity assumed that perfect estimates of current channel fading conditions are available at the

receiver. However, learning the fading coefficients becomes increasingly difficult as the number of transmitter antennas increase, especially for the frequency selective channels. Increasing the number of antennas increases the required training interval. In this paper, with the subspace method and the special structure of delay diversity, we propose the symbols detection method without the knowledge of channel. We address the symbol detection for a frequency selective channel from a single carrier perspective. With Monte Carlo simulations, we give the comparison of our algorithm with decision feedback equalization, which assumes that the channel information is known at the receiver.

WAM2L-219 -- Programable Logic Circuits

Wednesday: 10:40 am– 12:00 pm

Chair: Monte Tull

University of Oklahoma

WAM2L-219 -- The Circuit Designs of an SRAM Based Look-Up Table For High Performa nce FPGA Architecture

Prosenjit Mal, Jason Cantin, and Fred Beyette, *University of Cincinnati*

Look-up table (LUT) circuits are the core component of all Field Programmable Gate Arrays (FPGA¡¯s) architectures. Although considerable research has been done regarding the high-level architecture of different LUT¡¯s, very little has been done on the circuit-level description of the LUT. Though traditional LUT designs use NMOS transistors to implement pass-gates that save area and increase speed, large LUT designs require several pass gates in series. Unfortunately, multiple pass transistors in series will degrade the logic high level and thus jeopardize signal integrity. This paper explores different circuit-level implementations of the LUT circuitry with consideration towards the relative design trade-offs

WAM2L-219 -- A Fast Diagnosis Method for Interconnect Fault in FPGA

Yue Wang and Dongfang Liu, *Oklahoma State University*

With more and more widely uses of Field Programmable Gate Arrays (FPGAs), diagnosis of FPGAs becomes more and more important. In this paper, we present a novel method to quickly diagnose FPGA interconnect faults. By adding the maximum-length shift-registers in FPGA, all the testing configurations can be generated inside. The most time-consuming part of the testing, configuration bit-stream downloading, is not needed. Testing time is dramatically reduced. This testing time reduction advantage can be applied to any testing patterns.

WAM2L-219 -- Gigahertz FPGAs with New Architectural Ideas

Kuan Zhou, Channa Keshav, Russell Kraft, and John McDonald, *Rensselaer Polytechnic Institute*

The demand for high speed FPGAs has always been on a rise. This was never possible using CMOS as the basic device. People were able to achieve frequencies in the range of 70-250 MHz using CMOS. The availability of SiGe HBT devices have opened the door for Gigahertz FPGAs. Speeds over 5GHz were reported by B. S. Goda using SiGe 5HP technology. Using IBM's new 7HP technology, SiGe HBT devices with cutoff frequencies over 100 GHz can be fabricated. Apart from the improvement in device speed, architectural changes have been made to improve the speed and reduce the power. This paper is mainly going to elaborate on the architecture of the new SiGe FPGA and its advantages over the previous generation SiGe FPGA. The entire CLB has been implemented using 3 CML trees. The operating frequency of the new CLB is 10.4 GHz and the power consumption is "5.04 mW -sequential, 3.36 mW - combinational". Apart from these, 2 memory planes have been added to change the functionality of the FPGA dynamically. The original Widlar current mirror has been replaced by a CMOS current mirror which avoids the loading effect.

WAM2L-219 -- Predicting the Performance of FPGA Routing Algorithms

Li Gao, Brent Billups, and Carla Purdy, *University of Cincinnati*

Recent work on the NP-complete satisfiability problem (SAT) has revealed that commonly used heuristics for SAT may exhibit wildly unpredictable behavior for even small perturbations in input data. This type of behavior is unacceptable for algorithms which form the basis for modern VLSI CAD systems. We study the predictability of behavior for three well-known FPGA routing algorithms. Our results show that algorithm performance can vary unacceptably under reasonable input perturbations. Our study also gives insight in how to improve CAD system performance by providing optimization options to users.

WAM2L-221 -- Adaptive Signal and Image Processing II
Wednesday: 10:40 am– 12:00 pm
Chair: Guoliang Fan
Oklahoma State University

WAM2L-221 -- An Efficient Frame-based Signal Processing Algorithm

Yi Wan and Robert Nowak, *Rice University*

Frame-based signal processing promises to offer more adaptivity over methods based on regular orthogonal or biorthogonal bases. Current algorithms such as the method of frame (MOF), matching pursuit (MP), basis pursuit (BP) and translation invariant (TI) method achieve only limited success in practice. In this paper we propose a general efficient algorithm which outperform those methods in signal denoising. We also discuss its properties and extension.

WAM2L-221 -- Low SNR BPSK Signal Chip Rate Estimation Using A Wavelet Based Spectral Correlation Algorithm

Ying-Xiang Li, Min Yi, Qin Yang, and Xian-Ci Xiao, *UESTC,China*, and Heng-Ming Tai, *University of Tulsa*

The spectral correlation function (SCF) is an efficient tool for analyzing the BPSK signal. In a low signal-to-noise (SNR) condition, however, spectral lines associated with the BPSK signal chip rate in SCF may be corrupted by the quadratic characteristics of the SCF. By use of the quadratic property of SCFs and narrow-band characteristics of the BPSK signal, this paper proposes a wavelet transform (WT) based SCF algorithm to detect and estimate the BPSK chip rate in a low SNR environment. Examples are illustrated to validate the proposed method.

WAM2L-221 -- Design of Mixed-domain Filters for Detection of Arbitrary Trajectory Signals by Using Extended Complex Kalman Filters

Kazunori Maeda, Katsuya Kondo, Yasuo Konishi, and Hiroyuki Ishigaki, *Himeji Institute of Technology*

In this paper, we propose a novel method for the detection of objects moving with changing velocity vector with time in the transform/spatio-temporal mixed-domain (MixeD).The moving objects are considered as arbitrary trajectory signals (ATS).A trajectory signal in the MixeD is a bunch of 1-dimentional(1-D) complex signals.And an ATS is a bunch of quasi-periodic signals with pitch fluctuations in the MixeD.The proposed method is achieved by using a parallel bank of extended complex Kalman filters for the estimation of quasi-periodic signals.Experimental results show the feasibility of our approach.

WAM2L-221 -- Identification of Two Dimensional Harmonics via Polynomial Root Finding

Yibin Zheng, *University of Virginia*, and Shu-ming Tseng, *National Taipei University of Technology*

Identification and determination of parameters of two-dimensional harmonics are of special interest in signal processing theory, and has applications in source localization and joint angle/delay estimation for wireless

communications. For NxN samples, classical separable algorithms can identify only ~N harmonics. In this paper we present a closed form algorithm that can identify ~(N^2)/4 harmonics via 1-D polynomial rooting technique. Compared to other numerical solution techniques, the algorithm is both robust and computationally affordable. Numerical examples that validate the algorithm are also given.

WAM2L-223 -- Watermarking and Coding
Wednesday: 10:40 am– 12:00 pm
Chair: Edward Delp
Purdue University

WAM2L-223 -- Image Watermarking Using Wavelets
Peter Tay and Joebob Havlicek, *University of Oklahoma*

This paper proposes a novel image watermarking scheme. The technique uses a discrete wavelet transform to decompose an image into various frequency channels. A scaled watermark image is inserted into a wavelet channel. The non-zero scaling factor, the channel in which the watermark is inserted, and the wavelet can be encrypted and used as security keys for authentication. The proposed watermark extraction technique is independent of the original image. Experimental results provide a scaling factor which compromises between visually perceptible artifacts and resiliency in preserving the watermark image from various attacks.

WAM2L-223 -- A New Video Watermarking Protocol
Edward Delp, *Purdue University*

In this paper we will present some new results in watermarking video that has been compressed using scalable video compression.

WAM2L-223 -- Adaptive Digital Image Watermarking Using Singular Value Decomposition
Satish Chandra, *Kansas State University*

In this paper, we present a novel technique to embed watermarks imperceptibly in digital images based on the singular value decomposition (SVD). Watermark is embedded by computing the SVD of the entire image and also by performing block-based SVD. The energy compaction property and the ability of SVD to adapt to the variations in local statistics of an image will be utilized in embedding watermarks more efficiently. Simulation results are provided which demonstrate the robustness of the proposed technique to a broad range of image degradations. The results of our approach are also compared to other spatial and transform domain watermarking methods.

WAM2L-223 -- An Efficient Pyramid for Motion Vector Estimation
Jinwen Zan, M.Omair Ahmad, and M.N.S. Swamy, *Concordia University*

It is shown in this paper that by choosing an appropriate value for the parameter 'a' of the generating kernel in constructing Bert and Adelson's pyramid [1]for motion vector estimation, one can eliminate the operation of floating point multiplication needed in such a construction and reduce the computational load to the same order as in the case of the mean pyramid of [2]. It is further shown through simulation that this new kernel does not degrade the performance of the motion vector estimation, as compared to that using kernels giving the best performance.

WAM2L-225 -- MPLS, MPLambdaS, and GMPLS Networks II
Wednesday: 10:40 am– 12:00 pm
Chair: Harleen Chhabra
ExxonMobil

WAM2L-225 -- Traffic Engineering Based Optimal LSP Computation For MPLS Networks
Pravin Rasiah and Jong-Moon Chung, *Oklahoma State University*

This paper proposes an optimal routing scheme for routing LSP setup in the MPLS (MultiProtocol Label Switching)domain. RSVP-TE (Resource ReserVation Protocol ¨C Traffic Engineering) and CR-LDP (Constraint based Routed Label Distribution Protocol)used for LSP (Label Switched Path) setup usually use Source based routing schemes for routing them in the domain. The concepts presented in this paper support the delivery of traffic in accordance to the Traffic Engineering (TE) parameters (QoS, CoS, FEC, GoS, etc.) provided in the MPLS specifications. We also propose the use of Rate Controlled Service (RCS) disciplines in MPLS Label Switching Routers for providing QoS guarantees by determining the end to end performance characteristics from nodal analysis at each switch.

WAM2L-225 -- Handover Control and Analysis of WMPLS Networks
Sang-Chul Kim, Kannan Srinivasan, and Jong-Moon Chung, *Oklahoma State University*

This paper shows the handover protocol in the WATM and WMPLS. First, the handover differences of WATM and WMPLS is discussed. Then, the analytical derivations are calculated to understand the difference performance of two networks. To evaluate the two networks¡¯ performance, the handover delay and required buffer capacity is introduced.

WAM2L-225 -- MPLS-over-GRE Based VPN Architecture: A Performance Comparison
Ravi Bhagavathula and Ravi Pendse, *Wichita State University*

MPLS VPNs are one of the most widely deployed VPN architectures in the global Internet. However, a major pre-requisite for MPLS VPN is the support for MPLS in all the provider core routers. The situation becomes complicated when service providers themselves use a backbone carrier to bring connectivity to their networks since the ability of the backbone to support MPLS connectivity would be crucial to the service provider. MPLS-over-GRE tunnels is a new concept that has proposed to bring MPLS connectivity between networks that are connected by an IP-only network. The aim of the current paper is to evaluate the performance of MPLS Carrier Supporting Carrier configuration with and without MPLS-over-GRE tunnels.

WAM2L-225 -- Analysis of GMPLS Architectures, Topologies, and Algorithms
Jong-Moon Chung and Grace Cho, *Oklahoma State University*

Multiprotocol label switching (MPLS) and multiprotocol lambda switching (MPLambdaS) are at the forefront of next generation wide area network routing/switching technologies. Both technologies show promising functionalities and capabilities. While MPLS and MPƒÜS provide similar functions, they excel or show limitations in performance and services based on their inherent architectural designs and functional capabilities. A possible attempt of this kind may result from the ongoing development of Generalized MPLS (GMPLS) technology, but this is yet to be determined. With this focus, this paper investigates the similarities and differences of MPLS and MPLambdaS technology providing an analytical comparison within services, coverage, scalability, resource utilization, restoration speed/complexity, and blocking probability.

WAM2P-140 -- Neural Networks
Wednesday: 10:40 am– 12:00 pm
Chair: Roger Schultz
Halliburton Company

WAM2P-140 -- Multilayer Recurrent Neural Networks

H. K. Kwan, *University of Windsor*

In this paper, a multilayer recurrent neural network is presented. The network possesses the features of both a multilayer feedforward neural network and a recurrent neural network, has an improved performance for pattern recognition under noisy condition, and can be expanded easily to allow a larger storage capacity. This network can be trained to have two modes of recalling, namely, recalling by one pattern and recalling by a pattern pair. Simulation results are given.

WAM2P-140 -- Adaptive Neural Network Filtering Device for Enhanced Downhole Oilfield Measurements

Orlando De Jesus, DingDing Chen, Roger Schultz, and Jerry Foster, *Halliburton Energy Services*

Slickline(wireline)-deployed instruments are commonly used to perform measurement and service operations in oilwells. In order to accurately determine the downhole position of a suspended instrument, a device known as an electro-mechanical (EM) casing collar locator is sometimes used. The device is first lowered into a well and then slowly withdrawn. When a casing collar is encountered the EMCC device causes changes in the line tension. Changes in line tension measured at the surface are correlated to collar locations and hence instrument depth. Like many other applications, noise from different sources during slickline jobs may add contaminating noise or cause destructive interference in the monitored tension signals. In this paper, a method of using an adaptive neural network to filter the tension signal to remove unwanted noise is described. A theoretical discussion and the review of results of experimental testing are presented.

WAM2P-140 -- Robust Synthesis in l1 via m Approach and D-K iteration

Shing Tenqchen, *Chung-Hwa Telecom Labs,* Min-Chang Sun, *NTU,* Wu-Shiung Feng, *Chung-Gun University*, Lan-Da Van, *CIC*, and Bor-Sheng Jeng, *Chung-Hwa Telecom Labs*

In this paper, we propose the linear fractional transformation (LFT) method to synthesize controllers that achieve globally robust stability, robust performance, and worst-case performance, within any prescribed tolerance, against structured norm-bounded time-varying and/or nonlinear uncertainty, respectively. The uncertainty is characterized by any prescribed tolerance, against structured norm-bounded time-varying and/or nonlinear behaviors. The output feedback synthesis problem when the signal norm is proposed to get the norm and the perturbations are structured time-varying and/or nonlinear systems with an induced ¡Û-norm bound. A global optimal solution to the robust synthesis problem is obtained. A synthesizing l1 controller for a simplified space-shuttle model is taken from the m-Analysis and D-K Iteration method ([1], [14]) to compare the results of given example.

WAM2P-140 -- Control of Chaotic Heart Conditions Using Synchronization

Mohamed Sedky and Nadder Hamdy, *AAST*

Irregularity in heartbeats means that the heart becomes chaotic. To retain its normal pace, defibrillators or pacemakers are used. In this paper, synchronization using an artificial sensing system is suggested. A nonlinear mathematical model is used to construct a synchronization scheme that is capable of enforcing normal heart rhythm. Simulation results have demonstrated the effectiveness of the proposed technique in enforcing the heart to reassume a structurally stable limit cycle state. To confirm the results, a nonlinear equivalent circuit representing the describing equations has been designed and tested, which can lead to the development of future smart clinical pacemakers.

WAM2P-140 -- Optimal Synthesis of State-Estimate Feedback Analog Controllers with Minimum L2-Sensitivity

Takao Hinamoto and Takuya Inoue, *Hiroshima University*

An L2-sensitivity measure for the closed-loop system containing a state-estimate feedback analog controller is presented in closed form to evaluate the sensitivity of a closed-loop transfer function w.r.t. the state-estimate feedback controller's coefficients. This is accomplised by using a pure L2-norm. An iterative procedure is also developed for constructing state-estimate feedback controller's structures with minimum L2-sensitivity. Finally, a numerical example is given to illustrate the utility of the proposed technique.

WAM2P-140 -- Representation of Antenna Calibration Data Using Modular Neural Networks

Jason Niven and Keith Teague, *Oklahoma State University*

To perform accurate AOA (angle of arrival) estimations using the MUSIC (MUltiple SIgnal Classification) algorithm, accurate antenna array calibration data must be available. Since it is not feasible to store calibration data for all possible AOAs, developing continuous functions to represent the calibration data is an attractive alternative. Neural networks are effective for estimating functions, and are very applicable for this situation. Two different iterative training methods for modular networks are presented and compared. The first method employs a fixed section size and variable network size, and the second method employs a variable section size and a fixed network sized.

WAM2P-140 -- A New Neuro-based State Estimator

Mohammad Menhaj, *Oklahoma State University*

This paper presents a new neuro-computing approach to the problem of state estimation. The neuro-estimator is established by a hybrid combination of a Hopfield network and a feedforward multilayer neural net. The former is very useful for optimization and the latter is well-known for function approximation. This neuro-estimator is very appropriate for real-time implementation of nonlinear state estimators especially when modeling uncertainty is considered in the problem. The proposed estimator is applied to some practical problems to highlight its effectiveness.

WAM2P-140 -- Output Tracking Control of Nonminimum Phase Systems via Causal Inversion

Xuezhen Wang and Degang Chen, *Iowa State University*

This paper introduces a new design procedure for output tracking control of nonminimum phase systems. This new controller achieves stable epsilon-tracking of a reference profile given in real time via a causal inversion approach. Compared to stable inversion, causal inversion approach does not require precalculation. Compared to nonlinear regulation, the causal inversion avoids the numerical intractability of solving nonlinear PDEs and transient errors are significantly smaller. As an example, a causal inversion-based controller is designed for tip trajectory tracking of a one-link flexible manipulator. Simulation results demonstrate its effectiveness in output tracking.

WAM2P-140 -- Spiking Neural Networks for Biochemical Detection

Jacob Allen and Hoda Abdel-Aty-Zohdy, *Oakland University*

Artificial neural networks have proven to be a useful tool for olfactory pattern recognition; but most silicon-based implementations so far have been limited in scale due to inherent constraints on chip real estate and synapse routing. Additionally, silicon networks often have to be trained offline. Spiking networks may be the solution because they are suited to a scalable, digital architecture that economizes on chip space; with the bonus that they are a very close approximation to biological neural networks. Spiking networks implement on-line learning and statistically adjust their synapses to respond to changes in the environment. This paper discusses how spiking neural networks of linear integrate and fire neurons connected by two-state synapses could be

implemented for applications like bio-chemical detection. A new synaptic learning mechanism is presented that greatly simplifies hardware implementation. The new algorithm adjusts the synapse weights statistically based on the inter-spike interval of the pre and post synaptic neurons. This learning technique reduces the complexity of the stochastic synapse model proposed by Fusi, because learning becomes a function of neuron spike rates alone. This is especially beneficial for hardware implementation because the synapse circuit will not need to memorize any internal state. Using the reduced complexity synapse, the block diagram for an efficient digital network with many neurons and synapses is discussed. The circuit achieves the objectives of space economy, parallelism, scalability, synapse routing, on chip learning, and tight control over learning parameters. A general purpose, object oriented simulator has been developed for testing various spiking networks and their application to biochemical detection. A simulation of the proposed network and learning mechanism is tested to classify basic olfactory sensory inputs. Further results from this bio-inspired network may be developed to recognize complex scents from arrays of olfactory sensors.

WPM1L-209 -- Analog Filters III
Wednesday: 2:00 pm– 3:20 pm
Chair: TBA

WPM1L-209 -- Realization of (gm-C) Current Mode Filters from Associated (gm-C) Voltage Mode Filters

Rabin Raut and Srikanta Swamy, *Concordia University*

During the last decade a considerable amount of work has been done in designing current mode filters. Most of this has been based on designing a current mode filter from a voltage mode filter that uses a voltage amplifier. As early as in 1971, Bhattacharyya and Swamy defined an operation called Network Transposition, and showed how one could design a current mode filter directly from a given voltage mode filter. If the original voltage mode filter uses a voltage controlled voltage source, the corresponding transpose network would realize a current mode filter using a current controlled current source. However, if the If the original voltage mode filter uses a voltage controlled current source (VCCS), then its transposed network would realize a current mode filter using a VCCS, since the transpose of a VVCS is itself with its ports reversed. Thus, a voltage mode filter built with atransconductance amplifier (i.e., a gm-C filter) can be easily transformed into acorresponding (gm-C) current mode filter using the same VCCS as the active device. Simulation results using ideal ac equivalent models and macromodel of some practical transconductance (operational transcnductance amplifier OTA) devices have been obtained and will be presented in the symposium.

WPM1L-209 -- Wide-Tuning, Low-Voltage 1GHz Bandpass Filter Based on fT-Integration

Phanumas Khumsat, *Prince of Songkla University,* Apisak Worapishet, *Mahanakorn University of Technology,* and Alison Burdett, *Imperial College*

An integrated bandpass filter based on the fT-integration technique is experimentally demonstrated for the first time in GHz frequency range. The fT-integrator configuration employed offers enhanced performance compared to the originally introduced structure with lower supply voltage, more accurate frequency control and less chip area while still maintaining a wide frequency tuning capability. Fabricated in 0.8um-BiCMOS, the experimental filter obtains a centre frequency tuning over 200% (from 420MHz to 1320MHz) with -52dB THD for output current at 50% modulation index, 30dB spurious free dynamic range and 1dB-compression point dynamic range of 37dB at Q=14. The circuit operates at 1.8V-supply voltage with current consumption in each integrator varying from 1.9mA to 4.2mA for the entire tuning range.

WPM1L-209 -- CMOS Circuits for Thermal Asperity Detection and Recovery in Disk-Drive Read Channels

Aaron Lee, *AMD,* Paul Hurst, *University of California,* and Kiyoshi Fukahori, *TDK Semiconductor*

A thermal asperity detection and recovery scheme for a disk-drive read channel is presented. The circuit design and simulation results for two key blocks, the AC coupler and its tuning loop, in a 0.5um CMOS process are described.

WPM1L-209 -- A 0.8V filter based on a novel low voltage operational transresistance amplifier

Arun Ravindran, Anup Savla, Iqbal Younus, and Mohammed Ismail, *The Ohio State University*

Operational transresistance amplifier (OTRA) is suited for low voltage operation since it minimizes stacking of transistors due to the use of shunt-shunt feedback topology. A second order low pass filter with independent tuning of DC gain, cutoff frequency and Q factor was designed based on the Tow-Thomas biquad, using a novel low voltage OTRA in 0.18u CMOS technology. The filter operates at a supply of 0.8V, has a 3dB cutoff of 600KHz, VIP3 of 2.85V, input referred spot noise at 1KHz of 115nV/sqrt(Hz) and consumes 0.7mW power.

WPM1L-211 -- Dividers/Doublers and Prescalers
Wednesday: 2:00 pm– 3:20 pm
Chair: Rick Branner
Univeristy of California Davis

WPM1L-211 -- A High Gain 18 GHz Single Transistor Frequency Doubler
Jon Putnam and George Branner, *University of California, Davis*

This paper discusses the synthesis of microwave frequency multipliers in K band. These active devices have good conversion efficiency (>+2 db in the band of interest) and good unwanted harmonic rejection.

WPM1L-211 -- Fully Differential, High-speed Current-mode Controlled Dividers Designed Using Modular Approach
Md. Rahman and Syed K. Islam, *University of Tennessee, Knoxville*

This paper presents the technique of current mode switching in designing differential dividers for high-speed operation. Two dividers with fixed dividing ratios and a programmable divider are described to show the improvement in speed and noise performance by using current mode control and differential structure. Best performances can be obtained by optimizing parasitic. Dividers and logic gates have been designed in a modular fashion so that any dividing ratio can be obtained.

WPM1L-211 -- A Very Low Power CMOS, 1.5V, 2.5GHz Prescaler
Ahmad Mirzaei and Mojtaba Atarodi, *Sharif University of Technology*

A very low power and high speed prescaler was designed in 2.5GHz frequency range. It works with 1.5V power supply and dissipates about 1mW. Implemented in 0.25u standard CMOS technology, this prescaler can operate up to 3GHZ range.

WPM1L-211 -- Transient Analysis of Injection-locked Frequency Dividers
Ahmad Mirzaei and Mojtaba Atarodi, *Sharif University of Technology*

Injection locked frequency dividers (ILFD) are used for frequency division to reduce the overall power consumption. By injecting a high frequency signal to an LC oscillator, injecting signal gets synchronous with oscillator output. All ILFDs analysis reports are based on steady state solution when locking is reached. At the same time, it is important to consider transient analysis too. In this paper a simple model is developed to study phase transient analysis when injecting signal is small in amplitude. This model can be used for large signal injection as a good approximation.

WPM1L-213 -- Clock and Data Recovery Building Blocks
Wednesday: 2:00 pm– 3:20 pm
Chair: Jose Silva-Martinez
Texas A&M University

WPM1L-213 -- A 0.58 - 1Gb/s CMOS Data Recovery Circuit using a Synchronous Digital Phase Aligner
Taesik Cheung and Bhumcheol Lee *Electronics and Telecommunications Research Institute*

A data recovery circuit using a newly proposed synchronous digital phase aligner is realized for multi-link applications. The proposed circuit is implemented with 0.35um CMOS process technology. The experimental results show that the proposed circuit successfully recovers incoming 0.58 - 1Gb/s of 2^31-1 pseudo random bit sequence with less than 10^(-14) of bit error ratio.

WPM1L-213 -- A CMOS Phase/Frequency Detector with a high-speed low-power D-type Master-Slave Flip-Flop

Yubtzuan Chen, *Fengchia University*

An improved CMOS Phase/Frequency Detector (PFD) is presented. A high-speed low-power CMOS D-type master-slave flip-flop is proposed and adopted in the PFD. Higher speed and lower power operation are attributed to the reduced node capacitance. Charge-sharing phenomena are circumvented in the proposed PFD. The proposed PFD shows improvement in frequency sensitivity at high operating frequency. The improved PFD is suitable for high-speed low-power operation.

WPM1L-213 -- Jitter Analysis of a PLL-based CDR with a Bang-Bang Phase Detector

Mehrdad Ramezani and C. Andre T. Salama, *University of Toronto*

This paper provides a timing model to analyze the jitter generation of a Bang-Bang phase detector for PLL-based clock and data recovery (CDR) applications. Such a CDR is needed in the implementation of the serial data receiver in a broadband transceiver system. The input data is in Non-Return to Zero (NRZ) format. SPICE simulations are used to validate the analysis with particular emphasis on jitter generation caused by the bang-bang phase detector parameters.

WPM1L-213 -- A Novel Design for Deadzone-less Fast Charge Pumps with Low Harmonic Distortion at the Output

Behraad Bahreyni, *The University of Manitoba,* Igor Filanovsky, *The University of Alberta,* and Cyrus Shafai, *The University of Manitoba*

A novel design for a charge pump is presented. Unlike common charge pumps where the transistors are operating as switches, in this design transistors are kept in their saturation region at all times. This design has resulted in fast operation of the circuit in addition to lower levels of output current nonlinearities. A significant characteristic of this design is the smooth change of the output current which results in small spurious and phase noise levels if this charge pump is used in a PLL or frequency synthesizer. Comparison of simulation results for this circuit and those of a regular charge pump reveals the potential superiority of this design over traditional circuits.

WPM1L-214 -- Software Radio

Wednesday: 2:00 pm– 3:20 pm

Chair: Kathyayani Srikanteswara

Virginia Tech

WPM1L-214 -- System Analysis of a Multi-Standard Direct Conversion Wireless Receiver

Anup Savla, Arun Ravindran, Jennifer Leonard, and Mohammed Ismail, *Ohio State University*

Wireless devices with multi-mode function are gaining popularity, but existing multi-mode devices use separate chipsets, or separate receiver paths for different standards on the same chip. A multi-standard receiver with high level of hardware share between different standards is proposed. Measures to perform system analysis for the direct conversion architecture are analyzed and used in a Simulink model to extract design specifications for multi-standard receiver components.

WPM1L-214 -- Implementation of adaptive modulation on the Sunrise software radio

R. Michael Buehrer and Payal Jain, *Virginia Polytechnic Institute*

We shall investigate the implementation issues associated with adaptive modulation using pilot symbol assisted modulation based channel estimators for Rayleigh fading environments on the BAE System's Sunrise

receiver(C67). Sunrise has a download capability enhanced by the WJ-8629A developer's kit, which provides the end user the capability to create algorithms capable of addressing evolving requirements related to receiver filtering, demodulation, decoding and analysis. Modulation is adapted on the basis of the prevailing nature of the received signal SNR. Three switching levels for modulation schemes were fixed at to achieve a mean BER for QPSK, 16QAM, 64 QAM. Three different BER levels were investigated including 0.1%, 1% and 10%. We investigate the impact of channel quality estimation and observe crossovers in BER and spectral efficiency curves. We also examine the effect of frame delays on adaptive modulation. The full paper will present a more thorough presentation of the results.

WPM1L-214 -- Game Theoretic Analysis of a Network of Cognitive Radios

James Neel, Jeffrey H. Reed, and Robert Gilles, *Virginia Polytechnic Institute*

Cognitive radio is an enhancement on traditional software radio design where observations of the operating environment are combined with knowledge of the radio's available hardware and software capabilities to form decisions as to how the modify the radio's behavior to produce a desired level of performance. This paper will address how the insertion of cognitive radio technology into a network will impact performance. This paper will also demonstrate how techniques from game theory can be used to analyze and the network and shape the decisions of the radios to achieve optimal network performance.

WPM1L-214 -- A Programmable Baseband Processor Design for Software Defined Radios

Sridhar Rajagopal, Scott Rixner, and Joseph R. Cavallaro, *Rice University*

Future wireless systems need extremely fast and flexible architectures to support varying standards, algorithms and protocols with data rates in the range of 10-100 Mbps. A Software Defined Radio (SDR) based on DSPs is a widely proposed solution for these systems. However, SDRs designed with current generation DSPs do not provide real-time performance at these high data rates. We propose a programmable architecture solution for SDRs using a stream-based architecture based on the 'Imagine' media processor. The configurable 'Imagine' simulator allows us to investigate issues such as memory bottlenecks, number and type of functional units needed and their utilization. To evaluate stream-based architectures for baseband processing, we parallelize and implement sophisticated baseband algorithms such as multiuser estimation, multiuser detection and Viterbi decoding on this simulator. We present the features necessary in such a stream-based architecture to meet real-time constraints in SDRs. Comparisons with current generation DSP-based solutions show orders-of-magnitude performance improvements, both due to the stream-based nature of computations as well as the increase in the number of functional units having a high utilization factor. The result is a baseband processor designed with broad system functionality and flexibility that shows real-time performance potential for future wireless systems.

WPM1L-216 -- VLSI Systems, Design, and Simulation

Wednesday: 2:00 pm– 3:20 pm

Chair: K. Thulasiraman

University of Oklahoma

WPM1L-216 -- Modeling and Verification of a Pipelined CPU

Lubomir Ivanov, *Iona College*

In this paper we present a formal model of a pipelined version of the DLX processor, and verify the correct operation of the pipeline using a formal verification approach based series-parallel posets. We illustrate how the method can be used to detect pipeline hazard and other problems. The full verification was carried out automatically with the help of a verification tool, based on algorithms with low time- and space complexity.

WPM1L-216 -- Access Time and Energy Tradeoffs for Caches in High Frequency Microprocessors

Eugene John and Stefan Petko, *University of Texas San Antonio,* Lizy John and Jason Law, *University of Texas Austin*

This paper investigates the cache sizes and configurations that can be supported by a high frequency processor of the next generation. Based on the SIA roadmap prediction that a 0.1u processor of the next generation will run at 3.5GHz, we model caches of that technology using the CACTI tool. Access times as well as energy consumption are modeled for caches in the 8k-4M range, for various associativities. Impact of having multiple ports as well as that of varying block sizes is also studied.

WPM1L-216 -- Design of 0.18um CMOS Test Chip for Package Models and I/O Characteristics Verification

Chetan Deshpande and Tom Chen, *Colorado State University*

Reliable packages for modern chips are crucial for satisfactory system performance. Once the package is designed for the chip, in order to ascertain its performance, its equivalent electrical model is plugged into simulation decks and its performance characteristics analyzed. However, one implicit assumption designers make is that these equivalent electrical models are accurate for performance characterization of packages. Verification of the accuracy of these models is an objective of this design. Secondly, signal integrity for inter-chip communication is crucial from a systems perspective. To study the signal integrity of data under different PVT conditions, appropriate test structures are needed. Data can be subjected to controlled variations through these structures and its integrity studied. Design of such test structures to subject data to controlled variations have been proposed in this design. Thirdly, testing package reliability at high temperatures is important since on-chip temperatures are increasing dramatically as processes continue to scale. Modelling on-chip temperatures and studying thermal integrity of packages is a goal with this test chip. By analyzing the power supply droop on the test chip under different switching conditions and comparing it with the simulated data, the accuracy of package models can be verified. Furthermore, I/O cells on the chip have been custom designed to test signal integrity across the package and the transmission lines on the board. Additionally, the test chip has daisy chain structures that help analyze thermo-mechanical properties of the package under non-uniform distribution of heat across the die.

WPM1L-216 -- Computing the Noise Figure of Most Circuits by Applying Symbolic Analysis

Esteban Tlelo-Cuautle, *INAOE*

A method focused on computing the Noise Figure (NF) of MOS Transistor (MOST) circuits, is described. An important thing is that the NF is expressed as a symbolic function by applying symbolic analysis. In order to improve the time computation, a pure-nodal-analysis (PNA) is applied by modeling all the circuit elements using the nullor. The NF is computed either if the circuit works in voltage or current mode. Finally, after replacing all variables by their corresponding numerical value, a comparison with the simulation results from HSPICE is presented.

WPM1L-218 -- High Data Rate Modulation and Coding Techniques I

Wednesday: 2:00 pm– 3:20 pm

Chair: Matt Valenti

University of West Virginia

WPM1L-218 -- A High Data Transfer Rate Frequency Shift Keying Demodulator Chip for the Wireless Biomedical Implants

Maysam Ghovanloo and Khalil Najafi, *University of Michigan*

This paper describes a high-rate frequency shift keying (FSK) data transfer protocol and demodulator circuit for wirelessly operating biomedical implants in need of data transfer rates above 1Mbit/Sec. The demodulator circuit receives the serial data bit stream from an FSK carrier signal in 2~20MHz range, which is used to power the implant through inductive coupling. The circuitry has been designed and fabricated in the University of Michigan's single metal, dual-poly 3-mm CMOS process and has been tested fully functional.

WPM1L-218 -- Architectures and Implementations of Low-Density Parity Check Decoding Algorithms

Engling Yeo, Borivoje Nikolic, and Venkat Anantharam, *University of California, Berkeley*

Several architectures that have been proposed for low-complexity implementation of low-density parity check decoding algorithms are discussed. Use of serialized computations similar to traditional microprocessor-based decoding is compared against implementation with multiple processing elements that exploit the inherent parallelism in the decoding algorithms. Some interesting classes of LDPC codes, such as those based on irregular random graphs and on the geometric properties of finite fields, are evaluated along these lines in terms of complexity of implementation and performance. Issues of area and power consumption of the implementation are emphasized.

WPM1L-218 -- Beamforming for MC-CDMA systems

Michael Buehrer and Ramasamy Venkatasubramanian, *Virginia Polytechnic Institute*

MultiCarrier CDMA (MC-CDMA) has recently become a very popular technique for fourth generation wireless communications and is a useful technique for high data rates. Adaptive Beamforming with antenna arrays has been proposed for effective interference mitigation without allocating additional spectrum. In this paper we study the use of adaptive antenna arrays for MC-CDMA systems in an interference-dominated environment. Simulations were performed with different beamforming algorithms like MMSE-DMI, MSINR and MSNR in presence of Interference. The effect of channel estimation on the beamforming algorithm's performance is also investigated. Beamforming performance in different channel conditions such as flat fading, frequency selective fading, low and high angle spreads and low and high Doppler spreads were studied.

WPM1L-218 -- High-Rate Coded OFDM with Channel Equalization

Don Gruenbacher and Ali Serener, *Kansas State University*

We consider the use of wideband systems for the fixed point-to-point transmission of coded data with low bit-error rate requirements. A system is defined which is based on OFDM transmission with PSK and QAM subcarrier modulation, error control coding using low-density parity-check (LDPC) codes, and channel equalization to reduce intersymbol interference from a fading channel. Tradeoffs between modulation parameters and equalization complexity are also discussed. High rate LDPC codes are considered for this system.

WPM1L-219 -- High Performance Arithmetic Circuits Architectures I

Wednesday: 2:00 pm– 3:20 pm

Chair: Mohamad Farooq

Royal Military College of Canada

WPM1L-219 -- Tapered Transmission Gate Chains for Improved Carry Propagation

Boris Andreev, Edward Titlebaum, and Eby Friedman, *University of Rochester*

Carry propagation chains are commonly found along the critical paths of many digital VLSI systems and, in particular, arithmetic circuits. The carry propagation delay, therefore, has a significant effect on system performance. Innovative design approaches, such as carry-lookahead adders and redundant arithmetic, trade off area, delay, and power through shorter carry-propagation paths. The focus of this paper is on an alternative and complementary solution for decreasing the carry-propagation delay, particularly for those cases where transmission gate chains are used. The application of transmission gate chain tapering, supported by simulation results, is presented. With this proposed circuit technique, the area, delay, and power of the carry propagation chain may be significantly improved.

WPM1L-219 -- Implementation of Unidirectional Cordic Algorithm Using Precomputed Rotation Bits

Vijayan Asari and Satish Ravichandran, *Old Dominion University*

Design of a high-speed arithmetic unit with trigonometric computation has gained significant importance today. CORDIC is one such iterative algorithm that computes various trigonometric, logarithmic and transcendental functions fast with high degree of accuracy. This paper proposes a new technique to compute these values with significant reduction in the number of iterations and power savings. The conventional CORDIC technique is achieved by rotating a vector in both counter-clockwise and clockwise directions. The proposed technique uses unidirectional rotation of the vector thereby reducing the complexity of the circuit and also the number of iterations. Tests were conducted to compute the sine and cosine values using both the conventional and the proposed approach and the results show almost insignificant error (~10-8). This algorithm can be further used dominantly in any signal processing applications. An analytical treatment on the algorithm and the architecture is given in this paper.

WPM1L-219 -- High-speed Hybrid Threshold-Boolean Counters and Compressors

Marius Padure, Sorin Cotofana, and Stamatis Vassiliadis, *Delft University of Technology*

In this paper we propose high-speed hybrid Threshold-Boolean logic counters and compressors employed in parallel multiplication and multiple operand addition. First, we present a depth-2 hybrid implementation scheme for arbitrary symmetric Boolean functions, based on differential Threshold logic gates as circuit style. Subsequently, we apply the previous general scheme to parallel p/q counters and p|2 compressors. Finally, we present hybrid logic designs of a 7/3 counter and a 7|2 compressor. The simulation results, suggest that the hybrid 7/3 counter and 7|2 compressor, designed in .25um CMOS, achieve between 61% and 53% higher speed when compared with traditional full-adder based and Threshold logic counterparts, at expense of between 67% and 74% more transistors while having a regular routing.

WPM1L-219 -- Low-Voltage Power-Efficient Adder Design

Martin Margala, Ronald Alonzo, Guoqing Chen, Brandon Jasionowski, Keith Kraft, Michelle Lay, Jim Lindner, Mikhail Popovic, and Jason Suss, *University of Rochester*

This paper presents results of a comprehensive comparative study of recently presented full-adder cells, examines their suitability in low-voltage low-power and high-performance applications and it proposes a design methodology for a low-voltage power-efficient full adder. The study and the methodology are based on a power supply range of 1.0V-1.8V in 0.18µm CMOS technology.

WPM1L-221 -- Adaptive IIR Filter

Wednesday: 2:00 pm– 3:20 pm

Chair: Neeraj Magotra

Texas Instruments

WPM1L-221 -- A Robust Algorithm for Identifying Different Types of Engine Misfires

Abedulah Alkhateeb and Manohar Das, *Oakland University*

This paper introduces a robust algorithm for engine misfire detection that can detect and identify different kinds of engine misfires under various speed and load conditions. The overall algorithm consists of two main steps. First, it employs a frequency domain pattern classifier to detect and identify the type of misfire, and then it utilizes a generalized likelihood ratio test to locate the misfire instances. This paper is primarily focussed on the first task only. Results of extensive tests on a six cylinder engine are presented.

WPM1L-221 -- A Novel Approach for Single Microphone Active Noise Cancellation

Neeraj Magotra, *EEDS/TI*

This paper presents a novel approach for subband feedback active noise cancellation. Wideband active noise cancellation systems often involve adaptive filter lengths with hundreds of taps. Using subband processing can considerably reduce the length of the adaptive filter. Conventional subband algorithms are generally based in the frequency domain and use at least 2 sensors. This paper presents a time domain algorithm for single sensor subband feedback ANC using relatively short fixed FIR filters to do the subband processing. The algorithm also adopts the weight constrained NLMS algorithm for feedback ANC.

WPM1L-221 -- A Fast Converging Algorithm For Sparse Echo Cancellation

Mehran Nekuii and Mojtaba Atarodi, *Sharif University of Technology*

This paper presents a novel method for network echo cancellation, based on a combination of NLMS and Proportionate NLMS (PNLMS) adaptive filtering algorithms. First, based on a rough analysis of PNLMS adaptation, we show why after its initial fast convergence, it slows down, also we show that PNLMS has a higher steady state error in fixed point implementation compared to the NLMS, then the method used to overcome these deficiencies, is presented, and then by showing some of the simulations, its improvement over PNLMS algorithm is shown.

WPM1L-221 -- A Data-Derived Quadratic Independence Measure for Adaptive Blind Source Recovery in Practical Applications

Khurram Waheed and Fathi Salam, *Michigan State University*

We present a novel performance index to measure the statistical independence of data sequences and apply it to the framework of blind source recovery (BSR) that includes blind source separation, deconvolution and equalization. This performance index is capable of measuring the mutual independence of data sequences directly from the data. This information theoretic; Quadratic Independence Measure (QIM) is derived based on Renyi's quadratic entropy estimated by a finite data length Parzen window using a gaussian kernel. Simulation results are presented to validate the performance of the proposed benchmark and compare it with other established benchmarks.

WPM1L-223 -- Low Sensitivity Digital Filter Designs

Wednesday: 2:00 pm– 3:20 pm

Chair: Domenic Ho

University of Missouri

WPM1L-223 -- A Double Binary-Tree FIR Filter Form and the Corresponding Low-Sensitivity IIR Bandpass/Bandstop Structure

Jeffrey Coleman, *Naval Research Laboratory*

An FIR filter comprising back-to-back binary trees, each using multiple-sample delay blocks, offers advantages (1) for rate-changing filters, (2) when block delays are especially hardware efficient, and (3) when replacing block delays with allpass sections to create an IIR filter. In the latter case, the peak group delays of the allpass sections approximate the several distinct delays of the blocks replaced. With allpass sections fixed, the combining weights are easily optimized.

WPM1L-223 -- Passive Digital Filters

H. K. Kwan, *University of Windsor*

A systematic approach for the realization of multi-output first-order and second-order passive digital filters is presented, from which any high-order low-pass, high-pass, band-pass, and band-stop digital filter can be implemented. The filter structure is constructed from passive one-port and two-port digital networks that leads to desirable properties of zero-input, constant-input, and forced-response stability under finite word length arithmetic implementation. Issues such as low sensitivity, low round-off noise, and sharp cutoff transition band designs will be addressed. The coefficient values of a passive digital filter can be computed directly from an analog filter table or by direct mapping with the coefficients of a desired digital filter transfer function.

WPM1L-223 -- One Structure for Efficient Narrow-Band Bandpass FIR Filters

Gordana Jovanovic-Dolecek, *University of California Santa Barbara,* and Javier Diaz-Carmona, *Tech. Institute of Celaya*

This paper presents a narrow-band bandpass FIR filter design with a small number of multipliers per output sample (NMPS). The proposed method is based on the use of the Pipelining/Interleaving (PI) technique within a quadrature modulation structure, where only one narrow-band lowpass filter is required. In order to reduce the NMPS, the narrow-band lowpass filter is designed with an Interpolated Finite Impulse Response (IFIR) filter. Then interpolating filter is implemented by using the Sharpened Cascade Integrator Comb (CIC) filter. This results in considerable reduction of complexity.

WPM1L-223 -- ARMA Lattice Digital Filters

H. K. Kwan, *University of Windsor*

In this paper, a minimal normalized one-dimensional ARMA lattice digital filter structure is presented, for the realization of any given one-dimensional recursive digital filter. The filter structure is minimal in terms of the numbers of parameters and delays, and exhibits a high degree of structural regularity and modularity. The proposed ARMA lattice digital filters share the same desirable properties of the well-known Gray-Markel's AR lattice digital filter. Results on the finite word length simulations of the filters are presented to illustrate their coefficient sensitivity and round-off noise properties.

WPM1L-225 -- Network Security I
Wednesday: 2:00 pm– 3:20 pm
Chair: Raymond Garcia
Georgia Tech Research Institute

WPM1L-225 -- Network Vulnerability Analysis
Sujeet Shenoi, *University of Tulsa*

Network Vulnerability Analysis

WPM1L-225 -- SS7 Network Security
Sujeet Shenoi, *University of Tulsa*

SS7 Network Security

WPM1L-225 -- Invisible Trojan: An Architecture and Implementation
Raheem Beyah, Michael Holloway, and John Copeland, *Georgia Institute of Technology*

In this paper we give an overview of different system-security tools, including several types of intrusion detection systems (IDSs) and host based detection tools. We also discuss, in detail, port scanning and the primary algorithm used in current port-scanning devices. In addition, we discuss the limitations in the current algorithms used in port-scanning devices and exploit these limitations by implementing an Invisible Trojan that can elude today's port scanners.

WPM1L-225 -- Quantizing the Throughput Reduction of IPSec with Mobile IP
Dnyanesh Khatavkar, Rena Hixon, and Ravi Pendse, *Wichita State University*

The demand for immediate access to information universally is increasing rapidly, leading to the desire for mobile access to the Internet. The Mobile Internet Protocol (Mobile IP) provides mobility to Internet users with some basic security features that are insufficient. Internet Protocol Security (IPSec) brings security to the network, but uses more bandwidth. The desire for mobility does not reduce the requirement for security and maximum throughput. The purpose of this research is to further examine the effects of different security algorithms on bandwidth in mobile scenarios. The results of the measurements of throughput with different security implementations can allow the users to balance security and bandwidth.

WPM1P-140 -- Signal Image Analysis and Speech Processing
Wednesday: 2:00 pm– 3:20 pm
Chair: Mary Kohler
Department of Defense

WPM1P-140 -- Nonlinear Analysis of EEG Signals
Liang Fang, Hao Yang, and Wei He, *Chongqing University*, and Heng-Ming Tai, *University of Tulsa*

Nonlinear electroencephalogram (EEG) analysis provides a possible means for studying the dynamical changes in cortical networks related to mental activity. In this study, the correlation dimension (D2) was employed to investigate the quantitative complexity of 40Hz EEG signals. In addition, an efficient method to select effective segments of EEG data by detecting the bursts of 40Hz EEG is presented. EEGs were recorded in 10 normal subjects under four conditions: (1) passive eyes closed; (2) mental arithmetic with eyes closed; (3) passive eyes open; (4) mental reasoning with eyes open. Results show that D2 increases during mental arithmetic with eyes closed and is significantly larger in the left brain than the right one on the condition of the mental reasoning with eyes open.

WPM1P-140 -- Detection of Defects in Textures with Alignment Error for Real-Time Line-Scan Web Inspection Systems

Ibrahim Baykal, *University of Windsor*, and Graham Jullien, *University of Calgary*

Hash functions are recently introduced as an extremely efficient method to calculate a mesure of deficiency on repeating textures. These hash functions generate one dimensional signatures of patterns and they are simple enough to fit into a medium size FPGA. Although these functions are immune to change in illumination and contrast, they require the texture to be perfectly aligned. Any angular misalignment causes these functions to operate incorrectly. In this paper, a new family of hash function and a new signature analysis method are presented to overcome this problem.

WPM1P-140 -- Discrete-Space Systems and Volterra Series Representations

Irwin Sandberg, *University of Texas at Austin*

We give a Volterra-series representation theorem for discrete-space input-output maps that are analytic. The theorem provides a bound on the error in approximating the series with its first p+1 terms. Examples are given to illustrate how the theorem can be used.

WPM1P-140 -- Texture Classification Using Discriminant Wavelet Packet Subbands

Nasir Rajpoot, *University of Warwick*

This paper addresses the issue of selecting features from a given wavelet packet subband decomposition that are most useful for texture classification in an image. A functional measure based on the Kullback-Leibler distance is proposed as a way to select most discriminant subbands. Experimental results show a superior performance in terms of classification error rates.

WPM1P-140 -- A Multistrategy Signal Pattern Classifier

Roshdy Youssif and Carla Purdy, *University of Cincinnati*

Signal patterns are intrinsic to many sensor-based systems. Here we present a multi-strategy signal pattern classifier MSPC that can identify large numbers of signal pattern classes with low classification cost. MSPC combines decision tree concepts, fuzzy rules, genetic algorithms and neural networks to achieve its goal. This combination provides powerful classification capabilities with great tuning flexibility for either performance or cost-efficiency. Fuzzy rules measure similarities between signal patterns. A genetic algorithm finds the best fuzzy classification rule. Neural networks aid the final classification step and allow noise elimination. Machine learning concepts are applied to set the overall algorithm parameters.

WPM1P-140 -- Timing Jitter in a 1.35-GHz Single-Ended Ring Oscillator

Chengwei Zhang and Leonard Forbes, *Oregon State Univesity*

In this paper, we have simulated the timing jitter due to device noise in a three stage single-ended ring oscillator, and a methodology to efficiently simulate timing jitter has been developed. Simulation result shows the variation of absolute jitter due to flicker noise has linear dependence on time, while for white noise, it has a square root dependence, which are consistent with accepted theory. Two important parameters cycle jitter, and cycle to cycle jitter used to describe jitter performance can be obtained from simulation. The methodology described in this paper is also applicable to other types of oscillators such as differential ring oscillators and LC oscillators, as well as other kinds of noise sources as power supply and substrate noise.

WPM1P-140 -- Face Recognition by Means of Template Matching in Frequency Domain - a Hardware Based Approach

Peter Rauschert, Anton Kummert, Marco Krips, and Yuri Klimets, *University of Wuppertal*

Facial images are used for automated user identification. Various algorithms are known for realizing this task. Since most of these methods are software based solutions, a hardware based design is of interest for special

applications. Compared to the most common algorithms, template matching in frequency domain will be shown to be the most suited algorithm. In the resulting solution, the mathematical operations are reduced to minimum expense. Furthermore, data compression is done by concentration on the relevant coefficients in fourier space. Determination of the minimum euclidian distance to one reference set of data gives the probability for a valid match.

WPM1P-140 -- A Nonlinear Method of Frequency Estimation in Noise

Alireza Karimi Ziarani, *Clarkson University,* and Adalbert Konrad, *University of Toronto*

A novel time-domain method of estimation of instantaneous frequency of signals under the influence of noise is presented. The methodology is exemplified by its application to the estimation of Doppler frequency shift which is encountered both in aerospace and biomedical engineering. The estimation method is a nonlinear adaptive algorithm which exhibits a high degree of immunity to both external noise and misadjustment of internal parameters while offering structural simplicity crucial for real-time applications.

WPM1P-140 -- Towards Robustness in Speaker Verification: Enhancement and Adaptation

Chakib Tadj and Marcel Gabrea, *Ecole de Technologie Superieure*

In this paper, we study the performance limits of a standard HMM speaker verification (SV) system in "adverse conditions" context using two real noises with different SNR level. Two different techniques are investigated: a) Adaptive noise cancellation represents one such potentially effective technique and refers to a class of adaptive enhancement algorithms based on the availability of a primary input source and a secondary reference source. b) Maximum Likelihood Linear Regression (MLLR) transformation which adapts the system to the new environment based on modifying the continuous densities of the HMM mixtures. We apply the MLLR to perform environmental compensation by reducing a mismatch due to additive noise effects. Experiments on 60 speakers Yoho corpus corrupted by different type of noises showed that the performance of the SV can approach the optimal performance with the noise cancelling technique and improves it by more than 6% with the MLLR method.

WPM1P-140 -- A Study on the Improvement of Speaker Recognition System by Voiced Detection

DongSung Shin, JongKuk Kim, and MyungJin Bae, *Soongsil University*

The effect of silence segment elimination on the improvement of speaker recognition system was investigated in this study. Speaker recognition system is a method to identify input speech of a speaker by the comparison of previously registered and the test speech. The performance of this system greatly depends on a preprocessing stage. The experiments on the extraction of speech segments from speech wave forms during the preprocessing stage were conducted to analyze the rate of recognition. A new measure was developed and proposed, based on the fact that the slope of a valley at the pitch point in speech wave forms is higher when the normalized AMDF was applied to the stationary and transition regions. Voiced segments were extracted from the speech wave forms. From the voice segments, then unvoiced segments were detected using the autocorrelation ratio for the adjacent samples at the front and rear regions of the voiced segments. The results of this study indicated that this proposed method increased the perception rate by approximately 2% but had little effect on recognition time.

WPM1P-140 -- A Robust Algorithm for Detecting Speech Segments Using an Entropic Contrast

Khurram Waheed, Kim Weaver, and Fathi Salam, *Michigan State University*

This paper addresses the issue of automatic word/sentence boundary detection in both quiet and noisy environments. We propose to use an entropy based contrast function between the speech segments and the background noise. A simplified data based scheme of computing the entropy of the speech data is presented. The entropy-based contrast exhibits better-behaved characteristics as compared to the energy-based methods. An adaptive threshold is used to determine the candidate speech segments, which are subjected to word/sentence

constraints. Experimental results show that this algorithm outperforms energy-based algorithms. The improved detection accuracy of speech segments results in at least 25 % improvement of recognition performance for isolated speech and more than 16% for connected speech. For continuous speech, a preprocessing stage of the proposed speech segment detection makes the overall HMM based scheme more computationally efficient by rejection of silence periods.

WPM1P-140 -- A Text-Independent Speaker Identification System Using PARCOR and AR Model

Chia-Hsiung Liu and Oscal T.-C. Chen, *Chung Cheng University*

In this work, we propose the partial-correlation (PARCOR) coefficients scheme to model the cross areas of the several cylinders from the vocal tract. By using the relationship of the acoustic impedance proportional to the reciprocal of cross areas, the ratios of cross areas between each neighboring cylinders are used to model a speaker¡¦s vocal tract. The autoregressive model (AR model) is performed on the speech residual signals that are produced from the inverse vocal tract transform based on the PARCOR to generate features. These features with the conventional features from the Mel-Frequency Cepstral Coefficient (MFCC) are used for the identification engine of the Gaussian Mixture Model (GMM). According to our computer analyses in the TIMIT speech database, the proposed system can yield better identification performance than the conventional approach.

WPM1P-140 -- Performance of Internet and CDMA Cellular Data for Voice Over IP

Edward Daniel and Keith Teague, *Oklahoma State University*

This paper considers the performance of a voice over IP (VoIP) application over a combination of dissimilar networks consisting of internet and CDMA cellular data segments. Performance statistics were collected empirically using a specially developed test program for the purpose of measuring network characteristics. The results indicate a high variance of latency in the cellular network segment probably due to RLP, making it unfavorable for VoIP.

WPM1P-140 -- Speaker Identification Employing Waveform Based Speech CODEC

Wasfy Mikhael and Pravinkumar Premakanthan, *University of Central Florida*

A novel approach for Automatic Speaker Identification (ASI) employing Waveform based signal representation in multiple domains is presented. The proposed approach involves two stages, namely, the encoding stage, and the decoding stage. During the encoding stage (training mode), mixed transform coding, in conjunction with split vector Quantization (MTSVQ) is employed to form representative codebooks for each speaker. During the decoding stage (running mode), the vectors that best represent the unknown input vector are selected to represent the speech vectors. A normalised matching accuracy measure is developed to evaluate the proposed algorithms performance. The resulting technique is consistently found to obtain enhanced ASI accuracy in comparison with the earlier approaches as vector quantization employing single transform domains.

WPM1P-140 -- On the Use of Wavelet and Fourier Transforms for Speaker Verification

Nabil Badri, Azzouz Benlahouar, Chakib Tadj, and Christian Gargour, *Ecole de Technologie Superieure*

In this paper, we investigate the use of the Wavelet Transform for text-dependent Speaker verification task. An extensive experimental framework have been conducted using several approaches: (a) a fixed structure Wavelet Transform, (b) an adaptive wavelets scheme according to a given criterion and finally (c) a best basis according to the best wavelets Packet Transform. A speaker dependent library tree has been built, corresponding to the best structure for a given speaker. Finally, (d) a fusion of information combining wavelets and Fourier. Experiments have been conducted using 60 speakers, extracted from Yoho Database and a phone-based HMM speaker verification system. Results have been compared with MFCC features.

WPM2L-209 -- Analog Filters IV
Wednesday: 3:40 pm– 5:00 pm
Chair: TBA

WPM2L-209 -- Characterizing Metastability and Jitter in CMOS Latch / Flip-Flop Used as a Digital Mixer

Ira Shankar, Steven Morris, and Chris Hutchens, *Oklahoma State University*

A novel low power silicon-on-insulator (SOI) CMOS digital mixer circuit that is small, fully integrable and easily implemented is presented. This circuit is for use in a microbalance counter circuit (MBC) that operates at temperatures up to 180 degrees Celsius for petroleum industry well logging applications and has a measurement acquisition time of 2.4 seconds and a frequency resolution of 59 nHz when measuring 7 MHz signals. The digital mixer circuit eliminates the need for an analog mixer and bulky, temperature sensitive low pass filter components. This paper will focus on modeling and analysis of the metastable behavior and measurement inaccuracy caused by input phase jitter of the digital mixer. There is a risk of miscount due to jitter in the input signals. This paper will explain how to model this risk and generate design parameters given the user's criteria for maximum risk of count errors.

WPM2L-209 -- Low Voltage High-Q VHF CMOS Transistor-Only Active Inductor

Apinunt Thanachayanont, *King Mongkut's Institute of Technology Ladkrabang*

This paper describes circuit topologies that are suitable for realising very high frequency transistor-only active inductor in CMOS technology. Based on a low voltage topology, a novel VHF CMOS active inductor is proposed. The proposed inductor can achieve high Q with minimum circuit complexity, thus minimizing noise and power consumption. Comparing to previously reported inductors, the proposed circuit achieves much higher Q for the same power consumption, noise and dynamic range.

WPM2L-209 -- Technological Limitations of Monolithic High-Frequency Oscillators in MOS and Bipolar Processes

Sreenath Thoka, Chao Su, and Randall Geiger, *Iowa State University*

In this paper, the topic of oscillator frequency limitations is explored. The negative resistance and the ring oscillator structures are considered to show how the maximum frequency of operation relates to the fT of the semiconductor process being used. The analysis of these structures leads to interesting results that address conventional wisdom.

WPM2L-209 -- Low Voltage Low Power CMOS Inductorless RF Bandpass Filter With High Image Rejection Capability

Apinunt Thanachayanont, *King Mongkut's Institute of Technology Ladkrabang*

A new design approach suitable for realising low-power low-voltage high-order RF bandpass filter is proposed. Using a low-voltage VHF CMOS active inductor based on the exploitation of the intrinsic device capacitance, a compact tuneable 2nd-order RF bandpass filter is realised by adding a series capacitor to the input port of the inductor. The proposed 2nd-order filter can be readily cascaded to realise a high-order filter with enhanced image rejection ability. High-Q second-, fourth- and sixth-order fully differential filters are realised in a 0.35-mm CMOS process, and HSPICE simulations show that the filters can operate at the 2.4-GHz ISM frequency band under a 2-V power supply voltage with about 1 mW power dissipation per pole.

WPM2L-211 -- References
Wednesday: 3:40 pm– 5:00 pm
Chair: Rick Branner
University of California Davis

WPM2L-211 -- Design of a 1-V Low Power CMOS Bandgap Reference Based on Resistive Subdivision

Kimmo Lasanen, Vesa Korkala, Elvi Räisänen-Ruotsala inen, and Juha Kostamovaara, *University of Oulu*

A design of a CMOS bandgap reference (BGR), for portable applications with medium accuracy, is described and the measurement results of the fabricated chips are presented. The output voltage of the reference is set by resistive subdivision. In order to achieve small area and low power consumption, n-well resistors are used. This design features a reference voltage of 750 mV with 1s variation of ± 10 mV (1.3 %) without trimming with supply voltage range from 1 V to 1.6 V and temperature range of -20 oC .. 50 oC measured from 10 samples. The maximum supply current is 4.5 uA and the area of the design is ~ 0.13 mm2 with a standard 0.35 um double-poly n-well CMOS process.

WPM2L-211 -- Low-Voltage, Supply Independent CMOS Bias Circuit

Zhiwei Dong, *Georgia Institute of Technology*

A simple CMOS circuit is reported for generating supply-voltage independent bias voltages and currents, down to a minimum supply voltage of 0.68V (VT+2VDSat). The circuit is compatible with digital processes. Supply interference is rejected by more than 70dB.

WPM2L-211 -- A Programmable Monolithic Temperature Logging Device

Godi Fischer, Sangmok Lee, and Michael Obara, *University of Rhode Island*

This paper describes the design and the implementation of a miniature archival temperature monitoring device. The complete system consists of two components: a micro-chip and a small 3V lithium battery with a charge of 30mAh. Due to the nature of the application, the tag will spend most of its time in a sleeping mode. The MOS devices constituting the continuously operating oscillator are operated in weak inversion and thus dissipate not more than 1.5uW. The power consumed by the remainder of the chip's circuitry is minimized through effective power management. The temperature sampling events are controlled by an application specific protocol, which will be imported from a host PC prior to tag's deployment. The chip's memory consists of static RAM and can hold a maximum of 1,024 temperature readings.

WPM2L-211 -- Predicting the Effects of Error Sources in Bandgap Reference Circuits and Evaluating Their Design Implications

Vishal Gupta and Gabriel Rincon-Mora, *Georgia Institute of Technology Analog Consortium, Electrical Engineering, Georgia Institute of Technology*

Errors that arise from tolerance variations and mismatches between devices severely degrade the performance of bandgap reference circuits, which are essential building blocks to all high-performance systems. All these error sources have been analyzed (and verified through SPICE) and their design implications have been addressed. It has been found that a mismatch in the current mirror is the dominant source of error in bandgap reference-type circuits. Further, it has been found that resistor mismatch, transistor mismatch, and current-mirror mismatch errors have a PTAT variation, while resistor tolerance error has a CTAT dependence –both PTAT and CTAT errors are eliminated by trimming the PTAT terminating resistor in a bandgap circuit, only at room temperature–. Resistor TC errors cannot be trimmed out and must therefore be carefully selected and designed.

WPM2L-213 -- Communications Sysytem Performance Analysis
Wednesday: 3:40 pm– 5:00 pm
Chair: Bon-Jin Ku
Oklahoma State University

WPM2L-213 -- Interarrival Jitter Analysis of Packet Switched Networks Deploying Differentiated Services
Jong-Moon Chung and Hooi Miin Soo, *Oklahoma State University*

A critical challenge for networking vendors and carrier companies is to be able to accurately predict and determine their network quality of services (QoS) based on the network architecture, configuration, topology, and protocol applied. In addition, due to the development of technologies like multiprotocol label switching (MPLS), generalized MPLS (GMPLS), and IEEE802.3z, the variation in QoS performance due the deployment of differentiated services is of great interest and importance. In this focus, this paper provides a theoretical analysis of interarrival packet jitter performance based on priority class assignment and network traffic levels.

WPM2L-213 -- An Efficient Digital Down Conversion Method For Multiple Wideband Signals
Rong Zhang, *UESTC,* Xian-Ci Xiao, *UESTC,* and Heng-Ming Tai, *University of Tulsa*

This paper presents an efficient digital down conversion method for multiple wideband signals. This technique can be used to down convert odd and even subband signals to base band with only one polyphase filter. We can change filter coefficients to receive odd subband signals and then double odd subband bandwidth to receive even band signals. On the other hand, we can keep filter coefficients unchanged and double even subband bandwidth to receive odd band signals.

WPM2L-213 -- Mismatch Effect on Noise Figure for WLAN Receiver
C. P. Chiang, K. P. Lei, W. W. Choi, And W. Tam, *University of Macau*

In this paper, the impedance mismatch effect of the low-noise amplifier (LNA) on a homodyne receiver noise figure (NF) is investigated. An approximation is derived for determining receiver noise subject to LNA mismatch effect alone. The proposed method facilitates the planning of modern receiver. In order to validate this method usefulness, a homodyne receiver example for WLAN IEEE 802.11b is simulated and the obtained results demonstrate good agreement between theory and simulation.

WPM2L-213 -- Performance Analysis of Interactive Concatenated Coding Applying Diversity Reception in Mobile Communication Systems
Jong-Moon Chung, Bon-Jin Ku, Whasil Lee, and Hammad Khan, *ACSEL and OCLNB Laboratories*

In this paper, a macroscopic diversity reception system model applying interactive concatenated coding is proposed.

WPM2L-214 -- Ultra Wideband Radio
Wednesday: 3:40 pm– 5:00 pm
Chair: Mike Buehrer
Virginia Tech

WPM2L-214 -- Performance Comparison of ES/TH/DS UWB Systems Based on Frequency Domain Processing and Time Domain Processing

Fang Zhu, Carl Nassar, and Zhiqiang Wu, *Colorado State Univesity*

Ultra-Wideband (UWB) has been considered one of the strong candidates for short-range, high-throughput wireless communications. Typically, equally-spaced, time-hopping and direct-sequence are three major UWB pulse positioning schemes. In this paper, we compare the BER peformance of all these three UWB communication systems in multi-path fading channel. We also propose a novel pulse waveform named Carrier Interferometry waveform based on multi-carrier implementation for UWB systems. Employing CI waveform, frequency-domain processing is used to exploit frequency diversity and improve the performance and throughput. We also compare the BER performance of all three UWB systems using proposed CI waveform and frequency-domain processing. Simulation results suggest that CI waveform and frequency-domain processing based UWB systems significantly outperform current time-domain processing based systems.

WPM2L-214 -- Range Extension in UWB

Nishant Kumar, David McKinstry, and Dr. R. Michael Buehrer, *Virginia Polytechnic Institute.*

UWB shows great promise for use in a number of wireless communications applications, however, due to the emissions limits set by the FCC, commercial systems are limited in range for high data rates. Assuming constant transmit power, different modulation and channel coding techniques increase the range of the system for a particular throughput. Using a Rake receiver, additional energy can be captured which can also be used to increase the range of the system. In the paper, different modulation schemes have been compared for throughput versus range. The effects of using channel coding in a system have been compared with an uncoded system. Finally, the effects of using a Rake receiver over a conventional receiver have been analyzed.

WPM2L-214 -- Issues in the Covertness of UWB

David McKinstry and Dr. R. Michael Buehrer, *Virginia Polytechnic Institute*

UWB communications systems show potential for use in medium range applications requiring covertness, such as battlefield communications. Very low power spectral density is required for modest data rates in an UWB system as compared to more narrowband systems, because the UWB signal is spread over such a large bandwidth. Several techniques can be used to increase the covertness of UWB systems. The effects of modulation, channel coding, and receiver design on covertness are examined in this paper. Covertness is quantitatively analyzed by the probability of detection by a hostile interceptor.

WPM2L-214 -- UWB Channel Impulse Response Characterization Using Deconvolution Techniques

Ali Muqaibel, *Virginia Polytechnic Institute,* Norris Nahman, *Picosecond Pulse Labs,* Sedki Riad and Brian Woerner, *Virginia Polytechnic Institute*

The impulse response of UWB Channels can be estimated by sounding the channel with pulses and measuring the received signal. Rather than approximating the impulse response with the received signal, different deconvolution techniques are used to extract the UWB channel response. Application of deconvolution techniques results in resolving components smaller than the duration of the sounding pulse. This "super-resolution" allows for more accurate measurements of the delay spread. Resolving more components should improve the design of the rake receiver. The impulse response for a UWB communication system allows for performance evaluation studies such as simulating the effect of pulse shaping.

WPM2L-216 -- VLSI Design for Applications
Wednesday: 3:40 pm– 5:00 pm
Chair: K. Thulasiraman
University of Oklahoma

WPM2L-216 -- HDL Synthesis and Simulation of Eight Bit DSP Based Micro-controller for Image Processing Applications
Rangarajan Parthasarathy, *Sri Venkateswara College of Engineering,* Rajapaul Perinbam, Kutraleeshwaran Ramesh, and Vaasanthy Krishnamurthy, *Anna University*

This paper deals with VLSI design and simulation of fast eight bit DSP based RISC micro controller for real time image processing applications. By exploiting inherent concurrency of two dimension recursive filters, Folded systolic architecture is designed and combined with HAVARD architecture.Due to pipelined features each instruction takes one clock period for execution. Apart from ALU, program memory (PRAM), data memory (CROM),four register banks, two stacks are incorporated in design. Control signals for folded architecture is generated in the HAVARD architecture of RISC processor. The folded architecture has seven column processors which are capable of handling forty-nine pixels in forty-nine clock periods. Each column processor has fixed point adder, multiplier, latch and enable pin. The core has been designed using Verilog as HDL with SPARTAN SQSVQ100 as target FPGA device. Waveform of functional simulation of core confirms the micro-controller's capability of having throughput rate of ONE PIXEL PER CLOCK PERIOD.

WPM2L-216 -- Design of A 1.8-V CMOS Frequency Synthesizer for WCDMA
Young-Mi Lee, Ju-Sang Lee, and Sang-Dae Yu, *Kyungpook National University*

This research describes the design of a fully integrated fractional-N frequency synthesizer for the LO in WCDMA using 0.18mm CMOS technology and 1.8 V single power supply. A designed fractional-N synthesizer contains the following components. Modified charge pump uses active cascode transistors to achieve the high output impedance. A multi-modulus prescaler has modified ECL-like D flip-flop with additional diode-connected transistors for small transient time and high speed. And a phase-frequency detector, integrated passive loop filter, a LC-tuned VCO having a tuning range from 1.584 to 2.4GHz at 1.8V power supply, and a higher-order sigma-delta modulator. Finally designed frequency synthesizer provides 5MHz channel spacing with ?22.6 dBc/Hz at 1MHz in the WCDMA band and total output power is 28mW.

WPM2L-216 -- An Investigation of Timing Jitter In Bipolar ECL Ring Oscillators
Xinyu Wang, Chengwei Zhang, and Leonard Forbes, *Oregon State Univesity*

Timing jitter is a concern in high speed digital circuits, the presence of timing jitter will degrade the system performance in many high speed applications, it is a critical design consideration in nearly every type of digital systems. In this paper, we have investigated the timing jitter in a BJT ECL ring oscillator, and we have shown BJT oscillators have lower jitter compared to their CMOS counterparts. As such silicon BJT and/or SiGe HBT ring oscillators are a potential choice for low jitter applications.

WPM2L-216 -- Signal Perception and Processing with Bio-Inspired Sub-Micro-Systems
Hoda Abdel-Aty-Zohdy, *Oakland University*

Fast, cognitive, and compact integrated systems for accurate perception and signal processing are necessary for communications, information dissemination, and real-time control. Bio-inspired systems utilizing neural networks (NNs) and genetic algorithms (GAs) are presented in this paper for: (1) Pattern discovery and optimization; (2) Connection admission control; (3) Network congestion control; (4) Efficient resource management; (5) Combined priorities and constrains of service control; and (6) Application specific adaptation of the network to optimize quality service for run time signal processing. The presented bio-inspired systems include continuous recurrent dynamic neural networks (RDNNs), with output neurons feedback and feed forward arrays for noisy signals, genetic algorithms pre-processing stage followed by reinforcement neural

networks (RNNs) for multi-user networks with variable priorities and constraints. Efficient communication applications require: (1) Compact, low cost, more diverse and versatile sensing materials and devices. (2) Intelligent signal processing and perception. (3) Smart and flexible information transmission. Bio-inspired integrated microsystems will thus provide affordable, reproducible, and reliable front-end instrumentation, components and subsystems.

WPM2L-218 -- High Data Rate Modulation and Coding Techniques II

Wednesday: 3:40 pm– 5:00 pm

Chair: Matt Valenti

University of West Virginia

WPM2L-218 -- Convergence of Iterative Decoding for Fixed-Point Implementations

William Ebel, *St. Louis University*

Algorithms are often implemented on special purpose chips for high-volume hand-held applications in order to reduce cost and power requirements. Such an implementation requires that real numbers be represented by fixed-point numbers which have an inherent finite resolution and limited dynamic range which results in a performance loss. This paper presents a perspective on how to analyze and configure an algorithm in order to minimize the performance loss. The iterative Log-MAP Turbo Decoder is analyzed and a fixed-point implementation method is presented.

WPM2L-218 -- Digital Chaotic DS-CDMA Communication System

Nabil Zakria and Abdelatif Elkouny, *Kent University*

The use of chaotic signals as spectral spreading sequences in direct-sequence spread-spectrum (DS/SS) leads to several improvements in communication security and noise elimination. This paper presents a new approach for the design of DS-CDMA system. A digital information signal is modulated using chaotic code shift keying (CSK). The chaotic generator, based on the Lorenz system is slightly modified in order to control the amplitude and frequency of the chaotic signal and synchronized the receiver and transmitter. The results presented show that the receiver is able to recover fully the transmitted information without any degradation and with high security.

WPM2L-218 -- An Analog Turbo Decoder for an (8,4) Product Code

Neiyer Correal and Joe Heck, *Motorola*, and Matthew Valenti, *West Virginia University*

This paper explores the concept of applying analog computing ideas to the implementation of iterative decoding hardware. Interest in analog computation is motivated by the natural capabilities of analog computers for dealing with systems featuring parallel processing and feedback loops. The remarkable speed and inherent power efficiency of analog integrated circuits open the door for the development of higher throughput ultra-low power consumption decoding circuits.

WPM2L-218 -- Time Delay Influence on the Performance of Adaptive Turbo Coded Modulation

Wu Shouhao and Song Wentao, *Shanghai Jiaotong University*

In this paper, the method of data fitting is applied to obtaining the BER expression for turbo coded modulation, and a fitting mathematical model is proposed, which resolve the problem that there is no exact BER expression for turbo coded modulation in performance analysis. With the time delay consideration, the performance of BER of adaptive turbo coded modulation is analyzed and simulated. The results show that adaptive turbo coded modulation is very sensitive to time delay; and in order to assure the target BER requirement the total time delay should be less than.

WPM2L-219 -- High Performance Arithmetic Circuits Architectures II

Wednesday: 3:40 pm– 5:00 pm

Chair: Mohamad Farooq

Royal Military College of Canada

WPM2L-219 -- High-Speed Complex Number Multiplier and Inner-Product Processor

Monte Tull, Guoping Wang, and Murad Ozaydin, *University of Oklahoma*

Complex number arithmetic computations are one of the key arithmetic components in modern digital communication and optical systems. Complex number multiplication and complex number inner-product play a unique role in these applications. In this paper, a complex-number multiplier and complex-number inner-product processor based on a Redundant Binary (RB) representation are presented. This work is an extension of a previous real fixed-point inner-product hardware design. With the proposed algorithms, the complex number multiplication is reduced to parallel RB multiplications, and the complex number inner-product is produced using a RB addition tree. This proposed inner-product processor can be reconfigured or controlled to perform different computations such as inner-product processing or parallel multiplies for real and/or complex numbers. The design results, not only in simplified arithmetic operations, but also in a highly parallel and simple architecture when compared with other methods.

WPM2L-219 -- Adiabatic 4-bit Adders: Comparison of Performance and Robustness against Technology Parameter Variations

Ettore Amirante, Agnese Bargagli-Stoffi, and Jürgen Fischer, *Technical University Munich*, Giuseppe Iannaccone, *Università degli studi di Pisa*, and Doris Schmitt-Landsiedel, *Technical University Munich*

A large number of adiabatic families have been proposed, but there exist only few partial comparisons and no methodical investigations of the robustness of such circuits. We compare different adiabatic logic families with respect to energy consumption, area occupation and frequency range, finding significant differences among them and a reduction of energy dissipation by a factor of 10 compared to standard CMOS. The effect of supply voltage scaling is investigated as well as the sensitivity to technological parameters, and it is shown that different effects due to interdie and intra-die variations of the threshold voltage can strongly affect the power dissipation.

WPM2L-219 -- Graph-based Optimization for a CSD-enhanced RNS Multiplier

George Dimitrakopoulos and Vassilis Paliouras, *University of Patras*

A novel hardware algorithm, architecture and an optimization technique for residue multipliers are introduced in this paper. The proposed architecture exploits certain properties of the bit products to achieve low-complexity implementation via a set of introduced theorems that allow the definition of a graph based design methodology. In addition the proposed multiplier employs the Canonic Signed Digit (CSD) encoding to minimize the number of bit products required to be processed. Performance data reveal that the introduced architecture achieves area-time complexity reduction of up to 55%, when compared to most efficient previously reported design.

WPM2L-219 -- A Novel Approach to Multiple Constant Multiplication Using Minimum Spanning Trees

Oscar Gustafsson and Lars Wanhammar, *Linkoping University, Sweden*

In this work a novel approach to multiple constant multiplication based on minimum spanning trees is proposed. Each required coefficient is assigned to a vertex in a graph. The vertices are connected with weighted edges, where each edge weight corresponds to the number of adders required to derive one of the coefficient from the previous. The graph can be used to solve for the minimum spanning tree, which leads to a realization with a small number of adders. The optimal minimum spanning tree can be found in polynomial time. It is also possible to add extra constraints to the spanning tree, such as limited out-degree (corresponds to fan-out) and limited tree height (corresponds to delay). These problems are harder to solve, but there are good heuristics available.

It is shown by simulation that the performance of the proposed algorithm is comparable with recently published algorithms.

WPM2L-221 -- Adaptive Signal Processing Applications

Wednesday: 3:40 pm– 5:00 pm

Chair: Victor DeBrunner

University of Oklahoma

WPM2L-221 -- Cascaded Structures for Blind Source Recovery

Khurram Waheed and Fathi Salam, *Michigan State University*

Blind Source Recovery (BSR) is an interesting autonomous (or unsupervised) stochastic adaptation problem that includes well-known blind adaptive problems of Blind Source Separation (BSS), Deconvolution (BSD) and Equalization (BSE). BSR has been a hot research pursuit during the last two decades due to its several potential applications. A number of outstanding research contributions have been made in this field, however the issues of application are still in their infancy. Most of the BSR algorithms have characteristics, which make them suitable for a particular subclass of problems. In order to develop a generalized source recovery framework and yet achieve optimal performance in all cases, there is a need to explore the possibility to blend several of these algorithms. In this paper, we approach this goal in the architecture domain by focusing on the use of cascaded structures for BSR. A discussion on the need, choice, possible forms and properties of such cascaded structures are the topic of this presentation. Some illustrative simulations have been included to highlight the advantages of the proposed structures.

WPM2L-221 -- Recursive Quadratically Constraint Least Squares Bias-Free IIR System Identification Via Variable Loading

Izzet Ozcelik and Izzet Kale, *University of West Minster,* and Buyurman Baykal, *Middle East Technical University*

The cost function based on the Equation Error (EE) criterion has a global minimum for the Infinite Impulse Response (IIR) adaptive system identification. However, the solution found by minimizing the Mean Square Equation Error (MSEE) is biased. In this paper, a recursive algorithm based on the Recursive Least Squares (RLS) implementation of the EE criterion with a quadratic constraint is presented to get a fast algorithm without bias. A recursion method called variable loading is embedded into the RLS update equations with the constraint to adapt the coefficients of the denominator. The speed of convergence is increased considerably without bias.

WPM2L-221 -- Steady State Analysis of the P-Power Algorithm for a Constrained Adaptive IIR Filter

Maha Shadaydeh and Masayuki Kawamata, *Tohoku University*

In this paper, we present the steady state analysis for an adaptive IIR Notch filtering algorithm based on the Lp normed minimization for the case when p=3 and the sinusoidal signal is contaminated with additive Gaussian noise. We first derive two difference equations for the convergence of the mean and MSE, and then give the steady state estimation bias and MSE. Stability issue based on the step size value is also discussed.

WPM2L-221 -- A Unified Framework for Multichannel Fast QRD-LS Adaptive Filters Based on Backward Prediction Errors

César Medina, Jose A. Apolinario Jr., and Marcio G. Siqueira, *Instituto Militar de Engenharia*

Fast QR decomposition algorithms based on backward prediction errors are well known for their good numerical behavior and their low complexity when compared to similar algorithms with forward error update. Their application to multiple channel input signals generates more complex equations although the basic matrix expressions are similar. This paper presents an unified framework for a family of multichannel fast QRD-LS

algorithms. This family comprises four algorithms --- two basic algorithms with two different versions each. These algorithms are detailed in this work.

WPM2L-223 -- Multi-Dimentional Filter Designs

Wednesday: 3:40 pm– 5:00 pm

Chair: Domenic Ho

University of Missouri

WPM2L-223 -- Two-Dimensional Fuzzy Median Digital Filters For Image Filtering

H. K. Kwan and Y. Cai, *University of Windsor*

In this paper, 2-dimensional fuzzy median digital filters are presented. The proposed fuzzy median digital filters have a combined edge preserving and noise reduction capability. These filters share the advantages of a median filter and a moving average filter while avoiding their disadvantages. Symmetrical and asymmetrical triangular functions with median and average center points are used as weighted window functions. Simulation results indicate that these fuzzy median digital filters can reduce impulse noise, Gaussian noise, and both impulse noise and Gaussian noise in images.

WPM2L-223 -- Plane Wave Filtering Using A Novel 3D Cone-Stop Filter Bank

Leonard Bruton and Santosh Singh, *University of Calgary*

A novel spatio-temporal three-dimensional (3D) Cone-stop Filter Bank is proposed having a highly selective cone-shaped stop band in 3D frequency space. The direction and band width of the cone may be independently controlled and adapted over space-time. Preliminary results are given, for the 2D fan-stop case, that demonstrate adaptive jamming of a broad band plane wave having a time varying direction of arrival.

WPM2L-223 -- Analytical Design of Frequency Scaled Asteroidal 2-D FIR Filters

Pavel Zahradnik and Miroslav Vlcek, *Czech Technical University*

Novel approach to the analytical design of frequency scaled asteroidally shaped two-dimensional FIR filters is presented. The design consists of two steps. In the first step, the basic fourfold symmetrical asteroidal 2-D FIR filter is designed. The design is based on the analytical contour approximation using the parametric representation of the contour. Closed form formulas for the approximation of the contour with asteroidal shape were derived. In the second step, the basic filter is scaled along both frequency coordinates. Closed form formula for the calculation of the impulse response of the scaled filter is presented. One example demonstrates both steps of the design procedure.

WPM2L-223 -- Realization of 2-D variable IIR digital filter structures with a small amount of calculations for coefficient update

Hyuk-Jae Jang and Masayuki Kawamata, *Tohoku University*

This paper proposes a 2-D variable IIR digital filter structure with a small amount of calculations for coefficient update. In the proposed realization method, the parallel allpass 2-D variable filter structure is modularized in order to reduce the number of first-order complex allpass sections. Then, one first-order complex allpass section is omitted from each complex conjugate allpass section pair by combining their complex conjugate output. By means of the proposed method, the variable structure with minimal hardware elements can be realized. Comparison of the amount of calculations of each variable structure shows that the proposed variable structure has a smaller amount of calculations for coefficient update than the original variable structure.

WPM2L-225 -- Network Security II
Wednesday: 3:40 pm– 5:00 pm
Chair: Raymond Garcia
Georgia Tech Research Institute

WPM2L-225 -- WAID: Wavelet Analysis Intrusion Detection

Raymond Garcia, *Scientific Atlanta,* James Cannady, *Georgia Institute of Technology Research Institute,* Matthew Sadiku, *Boeing Satellite Systems*

Current approaches to intrusion detection have been demonstrated to be relatively effective in identifying network attacks that occur sequentially from a single source. Those that are distributed over an extended period of time are particularly difficult for current intrusion detection approaches to detect. Numerous forms of network attacks can be temporally dispersed. Those that deny authorized users access to system resources can often be most effectively conducted by distributing them through time. Wavelet analysis intrusion detection (WAID) is achieved by treating state-realizeable protocols as discrete waveforms. WAID is offered as a multi-dimensional analysis approach to detecting temporally-spaced network attacks. Several applications are discussed along with a theoretical basis.

WPM2L-225 -- Counter Mode Encryption for FNBDT/MELP

Robert Sleezer, Josh Raymond, Jerry Brewer, and Keith Teague, *Oklahoma State University*

Counter mode encryption is the proposed method for encrypting Mixed Excitation Linear Predictor (MELP) data for the Future NarrowBanc Digital Terminal (FNBDT). Counter mode encryption employs an indefinite keypad generated by an encrypting function applied to a counter. The clear (unencrypted) data is exclusive-or-ed with next available key in the pad. When encrypted data is received, the clear data may be retrieved by exclusive-or-ing the encrypted data with the same key used for encryption. The benefits and drawbacks of implementing counter mode encryption for real time MELP audio applications are presented.

WPM2L-225 -- Modeling Network Attacks with Conceptual Structures

James Cannady, *Georgia Institute of Technology,* and Mike Little, *Telcordia Techologies*

Effective network security continues to be a complex and elusive goal for researchers and application developers. One of the factors that has contributed to the difficulty in preventing, detecting, and responding to network-based attacks is the lack of an accurate and expressive method of modeling network attacks. Useable attack models would provide an analytical foundation for a variety of security technologies and greatly improve upon existing ad hoc methods of representing network attack data. In this paper we present the results of a research effort involving the application of conceptual structures in the modeling of tactical wireless network attacks. Conceptual structures are a form of semantic network that represent knowledge in patterns of interconnected nodes and arcs. The expressiveness, modularity, and inherent inferential capabilities provided by conceptual structures make them a viable approach in the modeling of complex network activity. The paper includes an overview of how these graphs can be applied to attack modeling and how these models can improve the ability of intrusion detection systems to infer the presence of complex network attacks.

WPM2L-225 -- Simultaneous Identity Verification and Membership Proof

Jian Ren, *Avaya Communication,* and Shervin Erfani, *University of Windsor*

An algorithm is given, which can verify a user's identity and his simultaneous membership in any groups that he has signed. The algorithm is proved to be secure and easy to implement. It can be used in smart cards, computer networks for identity verification and membership proof.

WPM2P-140 -- Microwave and Optical Systems and Synthesizers

Wednesday: 3:40 pm– 5:00 pm

Chair: Chia-Ming Liu

Oklahoma State Univerwity

WPM2P-140 -- A Novel Architecture for Integrated CMOS Wideband PLL-based Frequency Synthesizer

Haiyong Wang, *Tsinghua University*, Min Lin, *Tsinghua University*, Yongming Li, *Tsinghua University*, Hongyi Chen, *Tsinghua University*

Conventional CMOS frequency synthesizers have limited tuning range. A new structure for integrated wideband PLL- based frequency synthesizer is presented. The largest achieved tuning range is depended on the largest available voltage in a system. A prototype, which is the integer-N PLL-based frequency synthesizer, is designed and simulated using the TSMC 0.18um CMOS RF model. The tuning range at center frequency 1.1GHz is more than 250MHz when the available largest power supply is 3V.

WPM2P-140 -- A 1.35 GHz CMOS Wideband Frequency Synthesizer For Mobile Communications

Esdras Juarez-Hernandez and Alejandro Diaz-Sanchez, *National Institute for Astrophysics, Optics and Electronics*

The design and simulation of a 1.35 GHz CMOS frequency synthesizer for a double band receiver is presented. The proposed synthesizer is based in a wideband PLL topology with a high frequency reference, giving as result low phase noise, fast switching time, a low divider ratio and a reduction in the chip area. Besides, the use of a novel charge-pump circuit with positive feedback and current reuse allows a further reduction in both, chip area and power consumption, making the structure desirable for high-frequency low-voltage phase-locked loops.

WPM2P-140 -- Experimental Performance of a Coherent Communication System Based on Hyperchaos Synchronization

Damon Miller, Bradley Bazuin, and David Kerr, *Western Michigan University*, and Giuseppe Grassi, *University of Lecce*

An electronic realization of an antipodal hyperchaos shift keying communication system described in [Kolumban and Kennedy, 2000] has been constructed. The design is based on a linear observer circuit for a hyperchaotic oscillator as presented in [Miller and Grassi, 2001]. This paper will provide a comparison of simulated and experimental results and evaluate the potential of this observer technique for providing synchronization in coherent chaotic communication systems.

WPM2P-140 -- Configurable Architecture for Smart Pixel Research

Arvind Chokhani, V Sathya Vagheeswar, Shankar Raman Krishnakumar, and Beyette Jr. Fred, *University of Cincinnati*

The microprocessor industry has been striving hard to keep pace with the Moore's law. Two principal problems have been the interconnect delay and wiring density. This paper presents a new & efficient design, implementation of a 4x4 array of single-bit Optical RISC processors, demonstrating distribution of data through integrated CMOS photodetector and photoreceiver circuit. The CASPR chip incorporates an Instruction Fetch Unit (IFU) to provide instructions in correct sequence to Processing Elements(PEs) while taking care of branching. Each PE consists of Control Unit, Data path, ALU and Memory Register Bank and uses predication for conditional instruction execution.

WPM2P-140 -- Data Rate Enhancement of VDSL via Termination Impedance Matching

Martin Schwan and Joseph LoCicero, *Illinois Institute of Technology*

Impedance mismatch due to bridge taps is a data rate limiting factor in DSL systems including VDSL. Three impedance matching approaches are investigated for VDSL transmission through twisted-pair subscriber lines. Mathematical modelling of heterogeneous twist-pair transmission lines is discussed and forms the basis for

termination impedance dependent received signal-to-noise ratio computations. Several subscriber line and bridge tap lengths are examined. Results indicate improvements in channel capacity up to 40\% for cables with bridge taps that produce detrimental in-band frequency nulls.

WPM2P-140 -- Power/Bit Optimization of Delta-Sigma ADCs Using Multi-bit Quantizers

Chris Hutchens and Chia-Ming Liu, *Oklahoma State University*

A model for the design of power/bit efficient single loop Delta-Sigma analog-to-digital converter (ADC) modulators is developed and validated. Further, we demonstrate and validate experimentally that for high dynamic range ADCs (14~20 bits), 2nd order systems with 3 to 4 bit quantizers are power per bit (power/bit) optimal. Due to the wide architectural selection in quantizers, the scaling between 1st and subsequent integrators, and the SNR objective of the ADC, there can be a modest freedom in the number of quantizer bits (B), the order (L), and the over-sampling-ratio (OSR) for low power ADC designs. In the final analysis, multi-bit quantizers are shown to always offer an advantage in improving power/bit performance in both single loop and MASH Delta-Sigma modulators.

WPM2P-140 -- General Purpose Fast Switching PLL IC for Frequency Synthesis

Juha Hakkinen and Juha Kostamovaara, *University of Oulu*

An integrated circuit implementation of the two-pulses speed-up method is presented and applied for the first time to a fractional-N type synthesizer. The circuit (2.8mmx3.3mm, 80mA/5V) containing the speed-up circuitry, a PFD and a charge pump was fabricated in a 12 GHz double-poly/double-metal BiCMOS process. The measured phase noise of an example RF-synthesizer (fout = 1.638 GHz and N = 126) is -102.3 dBc/Hz @ 10 kHz and the level of the spurious is below -67 dBc. Measurements of the speed-up circuitry show that the current pulse magnitude can be controlled by 7-bits and the charge error between two similar current pulses is ±0.27%.

WPM2P-140 -- A 5GHz, 1.5 Volt and very low-power CMOS frequency synthesizer for wireless communications

Ahmad Mirzaei and Mojtaba Atarodi, *Sharif University of Technology*

A 5GHz, 1.5 Volt and low power CMOS frequency synthesizer with LC-tuned VCO (voltage controlled oscillator) is presented. The synthesizer consists of an LC-tuned VCO, an injection-lock frequency divider, a very low power prescaler which brings 2.5GHz range frequency to 11MHz, a phase-frequency detector and charge-pump with improved architecture. Spiral inductors with Q-factor of 9 are used for the LC-tuned 5GHz VCO. A fixed frequency divider based on injection-locking phenomenon is used to bring 5GHz VCO frequency to 2.5GHz. Both VCO and injection-locked divider's oscillators are tuned with NMOS varactors with their bodies are grounded, resulting in about 700MHz tuning range. Implemented in 0.25u standard CMOS process, the synthesizer consumes only 13.5mW with a single 1.5V supply.

WPM2P-140 -- A Completely Integrated, Low Noise, Low Power CMOS Frequency Synthesizer for GSM Communications

Khurram Waheed, Keyur Desai, Parmoon Seddighrad, and Fathi Salam, *Michigan State University*

A low power 22-mW 900MHz Frequency Synthesizer (FS), with an on-chip LC-tuned voltage controlled oscillator (VCO) for GSM applications is presented. The synthesizer possesses several novel features that include a completely integrated structure, a low phase noise on-chip LC VCO, a low-power Dual-Modulus Divider (DMD) in CML topology, a compensated charge pump with balanced switching, an on-chip third order loop filter and a proposed relatively easy to implement fractional accumulator based frequency synthesis technique. The complete synthesizer achieves in-band phase noise characteristics better than -110 dBc/Hz at 100kHz offset. The channel switching time is less than 500us for a 25MHz frequency hop. The synthesizer is able to accommodate all 195 transmit and receive channels in the R-GSM band. The proposed architecture has been realized using the 0.5 um AMI C5N technology. The complete integrated synthesizer occupies less than 1500 x 700 um2 of die real estate

WPM2P-140 -- A ROM Based Fractional-N Frequency Synthesizer for Wireless Communications

Alaa Hussein and M. I. Elmassry, *University of Waterloo*

The wireless market has experienced an exponential growth over the past few years. To sustain this growth along with the increasing demands of new wireless standards the cost, battery lifetime, and performance of wireless devices must all be enhanced. With the advancement of radio frequency (RF) technology and requirement for more integration, new RF wireless architectures are needed. One of the most critical components in a wireless transceiver is the frequency synthesizer. It largely affects all three dimensions of a wireless transceiver design: cost, battery lifetime, and performance. The common approach to frequency synthesis design for wireless communication is to design an analog-compensated fractional-N phase-locked loop (PLL). However, this technique lacks of adequate fractional spurs suppression for third generation wireless standards. In this paper, a new ROM based sigma-delta PLL architecture is reported to enhance the above mentioned limitations. This architecture has all the benefits of the sigma-delta architecture in terms of fractional spurs reduction without its drawbacks like speed, power cost, and stability. This aids in fully integrating a high-performance PLL frequency synthesizer, and hence reducing cost. The use of this architecture is examined to give a close match to the regular sigma-delta architecture in terms of noise shaping and measured spectrum at the VCO output.

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Session codes break down as follows:

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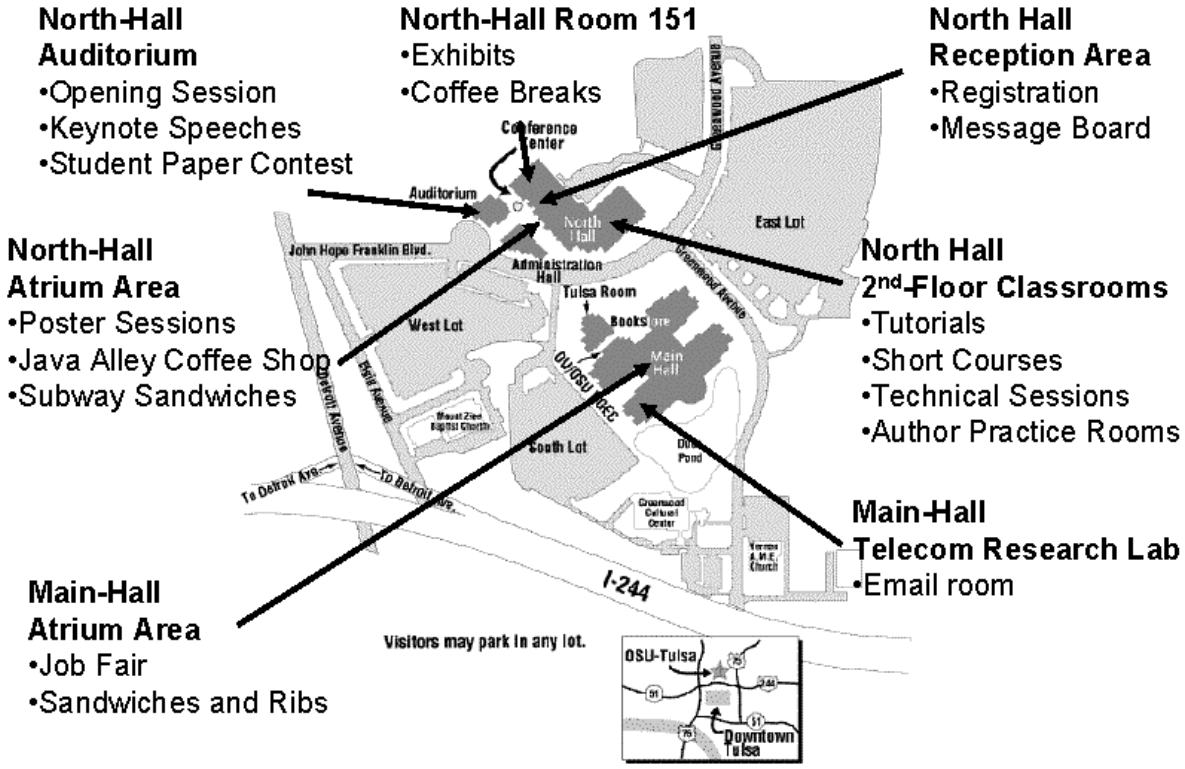

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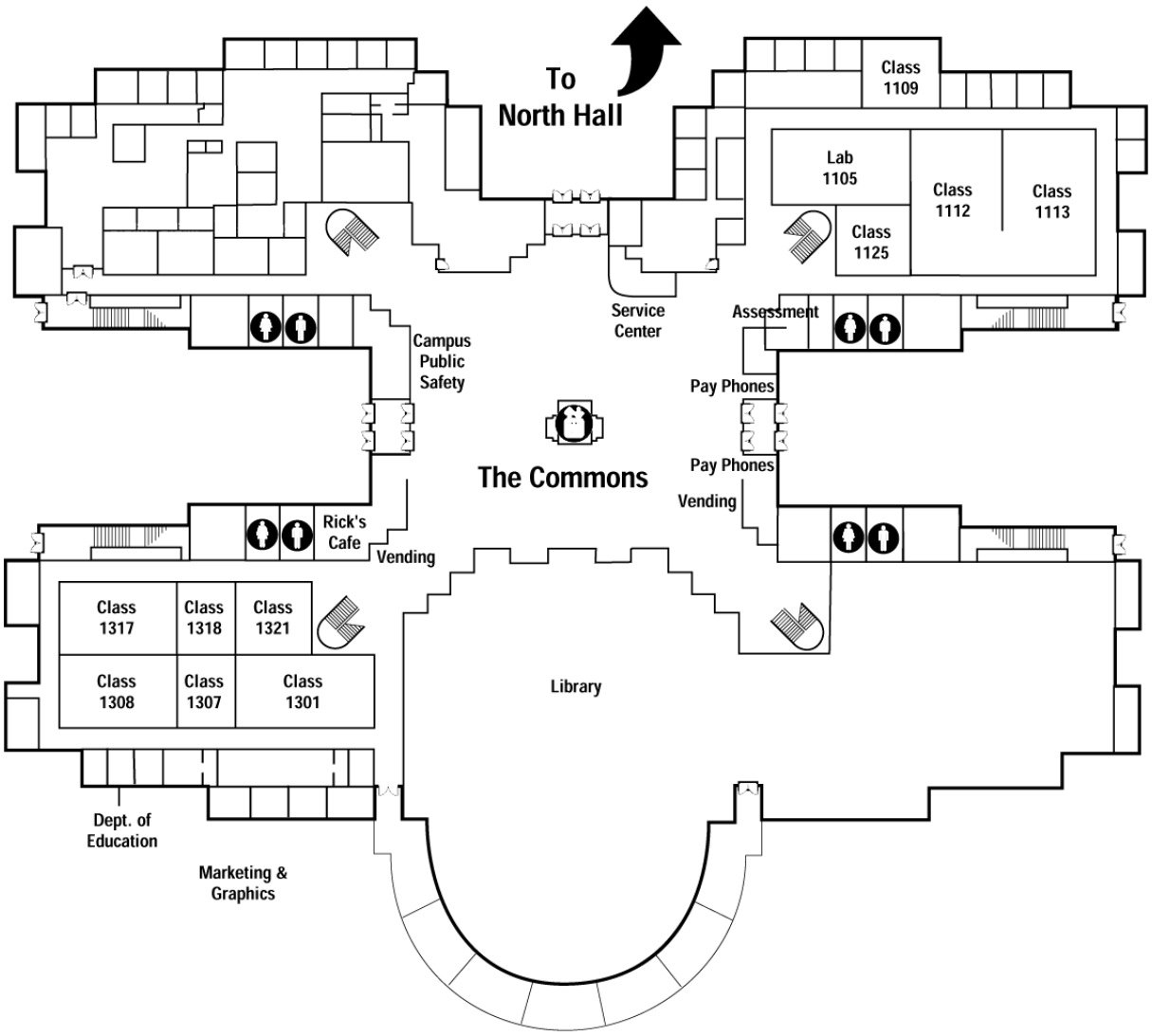
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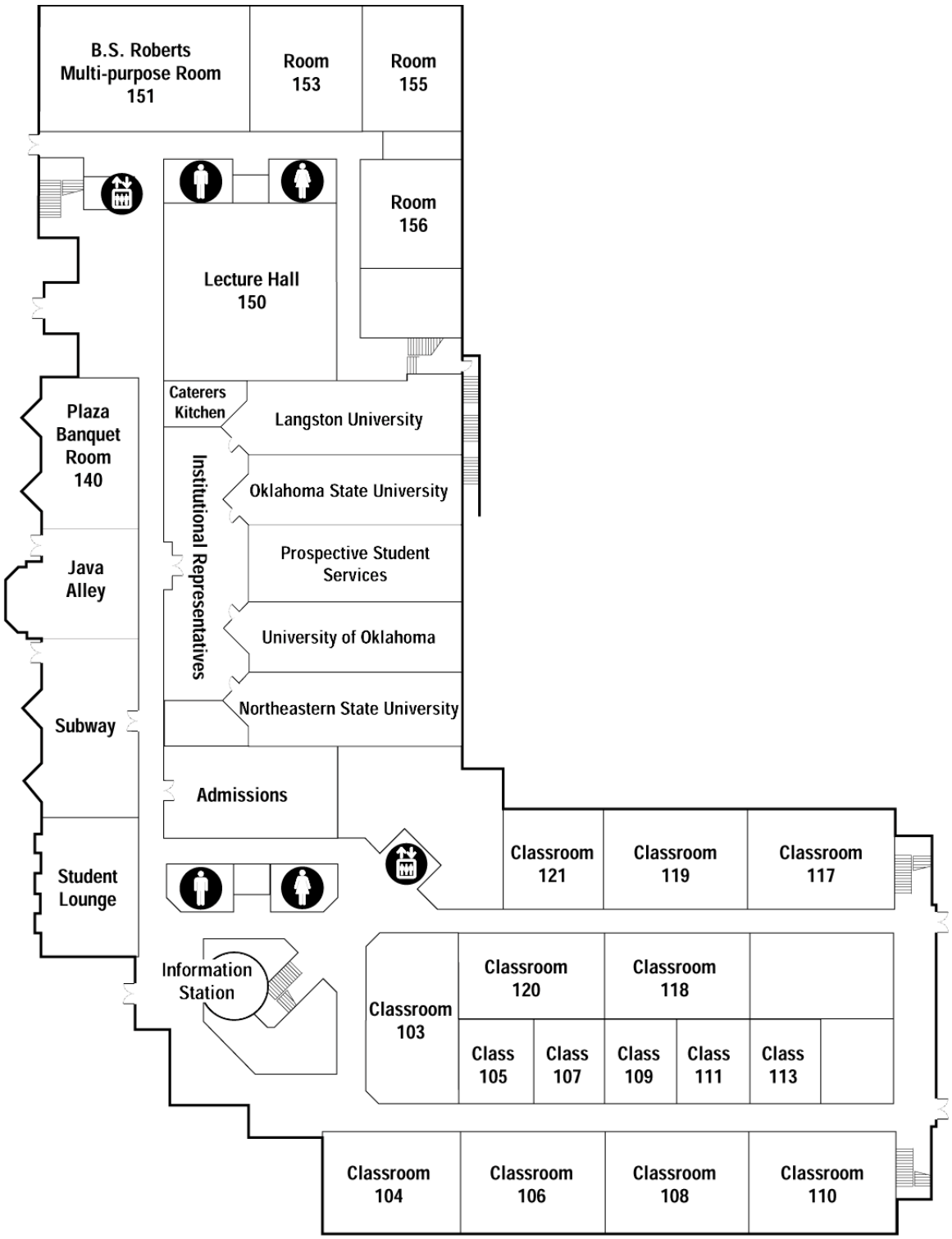

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